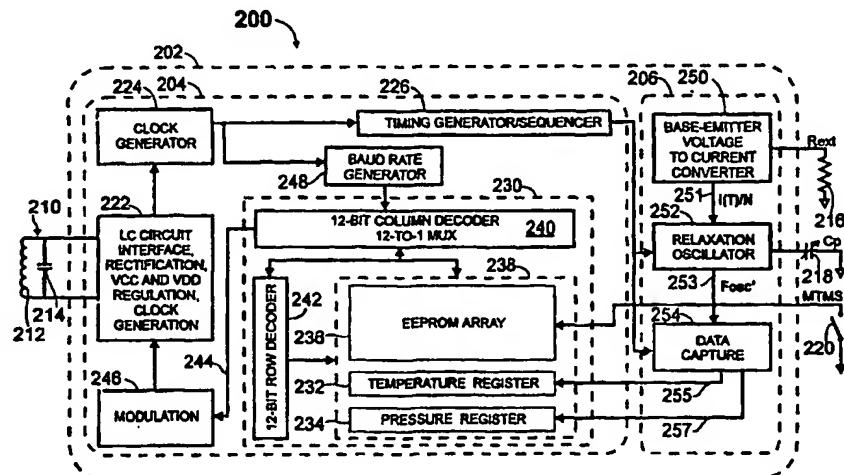




(51) International Patent Classification ⁷ : B60C 23/04		A1	(11) International Publication Number: WO 00/69663
			(43) International Publication Date: 23 November 2000 (23.11.00)
(21) International Application Number:	PCT/US99/29723		
(22) International Filing Date:	15 December 1999 (15.12.99)		
(30) Priority Data:	60/134,398	17 May 1999 (17.05.99)	US
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(54) Title: POWER-ON RESET FOR TRANSPONDER



(57) Abstract

A power-on reset for a transponder (102, 200, 400) capable of measuring one or more parameters (e.g., temperature, pressure) in an object (e.g., a tire, 104) and transmitting a data stream (Figures 3C, 4B) to an external reader/interrogator (106). The transponder typically operates in a passive mode, deriving its power (V_{xx} , V_{cc} , V_{dd}) from an RF interrogation signal received by an antenna system (210, 410), but can also operate in a battery-powered active mode. The transponder includes memory (238, 438) for storing measurements, calibration data, programmable trim settings (436b), transponder ID and the like. A power-on reset circuit (600) prevents operation of the transponder until it is stable, and starts transmission of the data stream at a first bit of the data stream, in order to ensure a first-pass transmission of a complete data stream. It also prevents modulation of the antenna system for data stream transmission if the power levels are too low for stable transponder operation during modulation.

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POWER-ON RESET FOR TRANSPONDER

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application relates to PCT applications entitled RELAXATION OSCILLATOR FOR TRANSPONDER, Attorney's Docket No. DN1999116PCT, PROGRAMMABLE MODULATION INDEX FOR TRANSPONDER, Attorney's Docket No. DN1999118PCT and PROGRAMMABLE TRIMMING FOR TRANSPONDER, Attorney's Docket No. DN1999256PCT, having a filing date concurrent with that of the present invention.

This application is a continuation-in-part of commonly-owned, copending US Provisional Patent Application No. 60/134,398, filed May 17, 1999 by Yones.

15 TECHNICAL FIELD OF THE INVENTION

The present invention relates to monitoring pressure and temperature and, more particularly in conjunction with transponders associated with the tires for transmitting pressure and temperature measurements to an external (e.g., on-board) receiver (reader, or reader/interrogator).

20 BACKGROUND OF THE INVENTION

Safe, efficient and economical operation of a motor vehicle depends, to a significant degree, on maintaining correct air pressure in all (each) of the tires of the motor vehicle. Operating the vehicle with low tire pressure may result in excessive tire wear, steering difficulties, poor road-handling, and poor gasoline mileage, all of which are exacerbated 25 when the tire pressure goes to zero in the case of a "flat" tire.

The need to monitor tire pressure when the tire is in use is highlighted in the context of "run-flat" (driven deflated) tires, tires which are capable of being used in a completely deflated condition. Such run-flat tires, as disclosed for example in commonly-owned USP 5,368,082, incorporated in its entirety by reference herein, may incorporate reinforced 30 sidewalls, mechanisms for securing the tire bead to the rim, and a non-pneumatic tire (donut) within the pneumatic tire to enable a driver to maintain control over the vehicle after a catastrophic pressure loss, and are evolving to the point where it is becoming less and less noticeable to the driver that the tire has become deflated. The broad purpose behind using run-flat tires is to enable a driver of a vehicle to continue driving on a deflated pneumatic 35 tire for a limited distance (e.g., 50 miles, or 80 kilometers) prior to getting the tire repaired,

rather than stopping on the side of the road to repair the deflated tire. Hence, it is generally desirable to provide a low tire pressure warning system within in the vehicle to alert (e.g., via a light or a buzzer) the driver to the loss of air pressure in a pneumatic tire.

To this end, a number of electronic devices and systems are known for monitoring the pressure of pneumatic tires, and providing the operator of the vehicle with either an indication of the current tire pressure or alerting the operator when the pressure has dropped below a predetermined threshold level.

For example, USP 4,578,992 (Galasko, et al; 04/86), incorporated in its entirety herein, discloses a tire pressure indicating device including a coil and a pressure-sensitive capacitor forming a passive oscillatory circuit having a natural resonant frequency which varies with tire pressure due to changes caused to the capacitance value of the capacitor. The circuit is energized by pulses supplied by a coil positioned outside the tire and secured to the vehicle, and the natural frequency of the passive oscillatory circuit is detected. The natural frequency of the coil/capacitor circuit is indicative of the pressure on the pressure-sensitive capacitor.

It is also known to monitor tire pressure with an electronic device which is not merely a passive resonant circuit, but rather is capable of transmitting a radio frequency (RF) signal indicative of the tire pressure to a remotely-located receiver. Such a "transmitting device" may have its own power supply and may be activated only when the pressure drops below a predetermined threshold. Alternatively, the transmitting device may be activated ("turned ON") by an RF signal from the remotely-located receiver, in which case the receiver is considered to be an "interrogator". Additionally, the transmitting device may be powered by an RF signal from the interrogator. Additionally, the electronic device which monitors the tire pressure may have the capability of receiving information from the interrogator, in which case the electronic device is referred to as a "transponder".

As used herein, a "transponder" is an electronic device capable of receiving and transmitting radio frequency signals, and impressing variable information (data) in a suitable format upon the transmitted signal indicative of a measured condition (e.g., tire pressure) or conditions (e.g., tire pressure, temperature, revolutions), as well as optionally impressing fixed information (e.g., tire ID) on the transmitted signal, as well as optionally responding to information which may be present on the received signal. The typical condition of paramount interest for pneumatic tires is tire pressure. "Passive" transponders are

transponders powered by the energy of a signal received from the interrogator. "Active" transponders are transponders having their own power supply (e.g., a battery), and include active transponders which remain in a "sleep" mode, using minimal power, until "woken up" by a signal from an interrogator, or by an internal periodic timer, or by an attached device. As used herein, the term "tag" refers either to a transponder having transmitting and receiving capability, or to a device that has only transmitting capability. Generally, tags which are transponders are preferred in the system of the present invention. As used herein, the term "tire-pressure monitoring system" (TPMS) indicates an overall system comprising tags within the tires and a receiver which may be an interrogator disposed within the vehicle.

It is known to mount a tag, and associated condition sensor (e.g., pressure sensor) within each tire of a vehicle, and to collect information from each of these transponders with a common single interrogator (or receiver), and to alert a driver of the vehicle to a low tire pressure condition requiring correction (e.g., replacing the tire). For example, USP 5,540,092 (Handfield, et al.; 1996), incorporated in its entirety by reference herein, discloses a system and method for monitoring a pneumatic tire. Figure 1 therein illustrates a pneumatic tire monitoring system (20) comprising a transponder (22) and a receiving unit (24).

Examples of RF transponders suitable for installation in a pneumatic tire are disclosed in U.S. Patent No. 5,451,959 (Schuermann; 09/95), U.S. Patent No. 5,661,651 (Geschke, et al.; 08/97), and U.S. Patent No. 5,581,023 (Handfield, et al.; 12/96), all incorporated in their entirety by reference herein. The described transponder systems include interrogation units, pressure sensors and/or temperature sensors associated with the transponder, and various techniques for establishing the identity of the tire/transponder in multiple transponder systems. In most cases, such transponders require battery power.

In some instances, a transponder may be implemented as an integrated circuit (IC) chip. Typically, the IC chip and other components are mounted and/or connected to a substrate such as a printed circuit board (PCB).

Some proposed systems have relatively complex transponder-sensor capabilities, including measurement and reporting of tire rotations and speed, along with tire ID, temperature, and pressure. For example: USP 5,562,787 (Koch, et al.; 1996), and USP 5,731,754 (Lee, Jr., et al.; 1998), incorporated in their entirety by reference herein.

TRANSPOUNDER ENVIRONMENTAL CONSIDERATIONS

The environment within which a tire-mounted transponder must reliably operate, including during manufacture and in use, presents numerous challenges to the successful operation of the transducer. For example, the sensors (e.g., pressure, temperature) used with the transponder preferably will have an operating temperature range of up to 125°C, and should be able to withstand a manufacturing temperature of approximately 177°C. For truck tire applications, the pressure sensor must have an operating pressure range of from about 50 psi to about 120 psi (from about 345 kPa to about 827 kPa), and should be able to withstand pressure during manufacture of the tire of up to about 400 psi (about 2759 kPa).
5 The accuracy, including the sum of all contributors to its inaccuracy, should be on the order of plus or minus 3 % of full scale. Repeatability and stability of the pressure signal should fall within a specified accuracy range.
10

However it is implemented, a tire transponder (tag) must therefore be able to operate reliably despite a wide range of pressures and temperatures. Additionally, a tire transponder must be able to withstand significant mechanical shocks such as may be encountered when a vehicle drives over a speed bump or a pothole.
15

A device which can be used to indicate if a transponder or the tire has been exposed to excessive, potentially damaging temperatures is the "MTMS" device or Maximum Temperature Memory Switch developed by Prof. Mehran Mehregany of Case Western Reserve University. It is a micro-machined silicon device that switches to a closed state at a certain high-temperature point. The sensor switches from an "open" high resistance state of, for example, over 1 mega-ohm to a "closed" low resistance state of, for example, less than 100 ohm.
20

Although it is generally well known to use pressure transducers in pneumatic tires, in association with electronic circuitry for transmitting pressure data, these pressure-data systems for tires have been plagued by difficulties inherent in the tire environment. Such difficulties include effectively and reliably coupling RF signals into and out of the tire, the rugged use the tire and electronic components are subjected to, as well as the possibility of deleterious effects on the tire from incorporation of the pressure transducer and electronics in a tire/wheel system. In the context of "passive" RF transponders which are powered by an external reader/interrogator, another problem is generating predictable and stable voltage levels within the transponder so that the circuitry within the transponder can perform to its
25
30

design specification.

Suitable pressure transducers for use with a tire-mounted transponder include:

- (a) piezoelectric transducers;
- (b) piezoresistive devices, such as are disclosed in USP 3,893,228 (George, et al.; 5 1975) and in USP 4,317,216 (Gragg, Jr.; 1982);
- (c) silicon capacitive pressure transducers, such as are disclosed in USP 4,701,826 (Mikkor; 1987), USP 5,528,452 (Ko; 1996), USP 5,706,565 (Sparks, et al.; 1998), and PCT/US99/16140 (Ko, et al.; filed July 7, 1999);
- 10 (d) devices formed of a variable-conductive laminate of conductance ink; and
- (e) devices formed of a variable-conductance elastomeric composition.

THE EFFECT OF TEMPERATURE ON GAS PRESSURE

In a broad sense, for a mass of any gas in a state of thermal equilibrium, pressure P, temperature T, and volume V can readily be measured. For low enough values of the density, experiment shows that (1) for a given mass of gas held at a constant temperature, 15 the pressure is inversely proportional to the volume (Boyle's law), and (2) for a given mass of gas held at a constant pressure, the volume is directly proportional to the temperature (law of Charles and Gay-Lussac). This leads to the "equation of state" of an ideal gas, or the "ideal gas law":

$$PV = \mu RT$$

20 where:

μ is the mass of the gas in moles; and

R is a constant associated with the gas.

Thus, for a contained (fixed) volume of gas, such as air contained within a 25 pneumatic tire, an increase in temperature (T) will manifest itself as an increase in pressure (P).

Because of the ideal gas law relationship, it is recognized that in the context of pneumatic tires, one problem that arises during operation of tire pressure sensors of any kind is that tires heat up as they are run for longer periods of time. When a tire heats up, air which is confined within the essentially constant and closed volume of the tire expands, thus 30 causing increased pressure within the tire, though the overall amount of air within the tire remains the same. Since the pressure nominally is different, a tire pressure sensor can provide different pressure readings when a tire is hot than would be the case if the tire were

5 cold. This is why tire and vehicle manufacturers recommend that owners check their tire pressure when the tire is cold. Of course, with a remote tire pressure sensor, an operator may receive a continuous indication of tire pressure within the vehicle, but the indication may be inaccurate because of the temperature change. Thus, it is necessary to compensate for changes in temperature of the inflating medium ("gas" or air) within the pneumatic tire.

Patents dealing in one way or another with gas law effects in pneumatic tires include:
10 USP 3,596,509 (Raffelli; 1971), USP 4,335,283 (Migrin; 1982), USP 4,126,772 (Pappas, et al.; 1978), USP 4,909,074 (Gerresheim, et al.; 1990), USP 5,050,110 (Rott; 1991), USP 5,230,243 (Reinecke; 1993), USP 4,966,034 (Bock, et al.; 1990), USP 5,140,851 (Hettich, et al.; 1992), USP 4,567,459 (Folger, et al.; 1986), all of which are incorporated in their entirety by reference herein.

15 USP 4,893,110 (Hebert; 1990), incorporated in its entirety by reference herein, discloses a tire monitoring device using pressure and temperature measurements to detect anomalies. As mentioned therein, a ratio of temperature and pressure provides a first approximation of a number of moles of gas in the tire, which should remain constant barring a leak of inflation fluid from the tire. (column 1, lines 18-26). More particularly, on each wheel are installed sensors (4) for pressure and sensors (6) for temperature of the tire, as well as elements (8 and 10) for transmitting the measured values as coded signals to a computer (12) on board the vehicle, such as disclosed in the aforementioned USP 20 4,703,650. The computer processes the measured values for pressure and temperature for each tire, and estimates for the pressure/temperature ratio (P/T estimate) are calculated for each wheel. Generally, the ratio for one of the tires is compared with the ratio for at least another one of the tires, and an alarm is output when a result (N) of the comparison deviates from a predetermined range of values.

25 **TECHNIQUES FOR TRANSMITTING PRESSURE AND TEMPERATURE READINGS FROM A TIRE**

Given that pressure and temperature conditions within a pneumatic tire can both be measured, various techniques have been proposed to transmit signals indicative of the measured pressure and temperature conditions to an external interrogator/receiver. For 30 example, the following patents are incorporated in their entirety by reference herein:

- transmit the signals individually, distinguished by phase displacements: USP 4,174,515 (Marzolf; 1979);

- multiplex the signals: USP 5,285,189 (Nowicki, et al.; 1994), USP 5,297,424 (Sackett; 1994);
 - encoding the signals as separate segments of a data word: USP 5,231,872 (Bowler, et al.; 1993), and USP 4,695,823 (Vernon; 1987) which also incorporates both the telemetry and the pressure and/or temperature sensors on the same integrated circuit chip;
 - transmission between coils mounted on the wheel and on the vehicle: USP 4,567,459 (Folger, et al.; 1986);
 - use a frequency-shift key (FSK) signal: USP 5,228,337 (Sharpe, et al.; 1993);
 - backscatter-modulate the RF signal from the interrogator with the tire condition parameter data from the sensors, then return the backscatter modulated signal to the interrogator: USP 5,731,754 (Lee, Jr., et al.; 1998).
- 10 USP 4,703,650 (Dosjoub, et al.; 1987), incorporated in its entirety by reference herein, discloses a circuit for coding the value of two variables measured in a tire, and a device for monitoring tires employing such a circuit. The coding circuit comprises an astable multivibrator which transforms the measurement of the variables, for instance pressure and temperature, into a time measurement. The astable multivibrator delivers a pulse signal whose pulse width is a function of the temperature and the cyclic ratio of which is a function of the pressure.
- 15 USP 5,054,315 (Dosjoub; 1991), incorporated in its entirety by reference herein, discloses a technique for coding the value of several quantities measured in a tire. As disclosed therein:
 - "Coding of the value of any number of quantities measured in a tire, for example its pressure and its temperature, is carried out using a ratio of time intervals TP/Tr , Tt/Tr . This frees the device from the effect of the time shift of the modulation system, the time shift affecting simultaneously the numerator and the denominator of said ratio." (Abstract)

SUMMARY OF THE INVENTION

According to an aspect of the invention, a radio-frequency (RF) transponder comprises circuitry capable of transmitting information unique to an object with which the transponder is associated to an external reader/interrogator. Additionally, one or more transponder sensors (transducers) provide real-time parameter measurement at the transducer location. These measurements are transmitted to the external

reader/interrogator, in the form of data in a data stream, on a signal which is output by the transponder, such as by impressing (modulating) the data stream onto an RF signal transmitted by the transponder to the external reader/interrogator.

According to an aspect of the invention, typically two real-time parameters are measured: pressure and temperature. Pressure is preferably measured by a separate ("off-chip") pressure sensor, which is of a type that varies its capacitance value in a known way, such as a polynomial, or preferably as a substantially linear function of ambient pressure. Preferably, the temperature sensor is embedded ("on-chip") in the IC chip of the transponder and disposed so as to be subject to substantially the same ambient temperature as the pressure sensor so that a true, temperature-compensated pressure can readily be calculated.

According to an aspect of the invention, the transponder comprises a Power-On Reset (POR) circuit for generating a reset signal for maintaining other ones of the transponder circuits in an inoperative reset mode unless the power supply has sufficient power to ensure proper operation of the circuits, and at least one of the other circuits being control logic which, upon release of the reset signal, starts transmission of a data stream at a first bit of the data stream, in order to ensure a first-pass transmission of a complete data stream.

According to features of the invention, circuitry is provided to hold the reset signal on for a delay time after abrupt or rapid power-up of the transponder. By comparing the transponder input voltage level to fixed reference voltages, the POR circuit sets the reset signal whenever the input voltage is less than or equal to a minimum sustaining voltage, and clears the reset signal whenever the input voltage is greater than the minimum sustaining voltage. By means of a logic switch controlled by a programmable trim setting, the minimum sustaining voltage can be different for different transponder operating modes, such as battery-powered (active) or RF signal-powered (passive) operation. The POR can be enhanced so that it sets the reset signal while the input voltage is increasing from less than or equal to a minimum sustaining voltage to a minimum starting voltage, and clears the reset signal whenever the input voltage increases above the minimum starting voltage; and so that after the input voltage has increased above the minimum starting voltage, the POR maintains a cleared reset signal state as long as the input voltage remains above the minimum sustaining voltage; and so that after the input voltage has increased above the minimum starting voltage, the POR sets the reset signal when the input voltage decreases to less than

or equal to the minimum sustaining voltage.

According to a feature of the invention, a combined reset signal is formed which is set whenever either an externally-supplied reset signal or the transponder-generated reset signal is set, and the combined reset signal is cleared only when both the external and the transponder-generated reset signals are clear. Furthermore, the externally-supplied reset signal can be cleared by transponder logic whenever the voltage level of the power supply is suitable for digital logic control.

According to a feature of the invention, the power for the POR circuitry generating and releasing the reset signal is the highest available regulated voltage, and the POR components are selected for minimal power use and for operation at the lowest possible voltages so that the POR circuitry is functional before the other transponder circuits. Such components include, for example, low current, three-stage comparators, Schmitt trigger inverters, and a low current voltage divider, utilizing on-chip, high value poly resistances.

Other objects, aspects, features and advantages of the invention will become apparent from the description that follows.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference will be made in detail to preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. The drawings are intended to be illustrative, not limiting. Although the invention will be described in the context of these preferred embodiments, it should be understood that it is not intended to limit the spirit and scope of the invention to these particular embodiments.

Certain elements in selected ones of the drawings may be illustrated not-to-scale, for illustrative clarity.

Often, similar elements throughout the drawings may be referred to by similar references numerals. For example, the element 199 in a figure (or embodiment) may be similar in many respects to the element 299 in an other figure (or embodiment). Such a relationship, if any, between similar elements in different figures or embodiments will become apparent throughout the specification, including, if applicable, in the claims and abstract.

In some cases, similar elements may be referred to with similar numbers in a single drawing. For example, a plurality of elements 199 may be referred to as 199a, 199b, 199c, etc.

The cross-sectional views, if any, presented herein may be in the form of "slices", or "near-sighted" cross-sectional views, omitting certain background lines which would otherwise be visible in a true cross-sectional view, for illustrative clarity.

5 The structure, operation, and advantages of the present preferred embodiment of the invention will become further apparent upon consideration of the following description taken in conjunction with the accompanying drawings, wherein:

Figure 1 is a generalized diagram of an RF transponder system comprising an external reader/interrogator and an RF transponder within a pneumatic tire, according to the prior art;

10 Figure 2 is a block diagram of major components of an RF transponder, according to a previous model of the invention;

Figure 3 is a schematic diagram of major portions of the RF transponder of Figure 2, according to a previous model of the invention;

15 Figure 3A is a schematic diagram of a portion of the RF transponder of Figure 2, according to a previous model of the invention;

Figure 3B is a schematic diagram of a portion of the RF transponder of Figure 2, according to a previous model of the invention;

20 Figure 3C is a diagram of a memory space within the RF transponder of Figure 2, illustrating how data may be arranged and transmitted, according to a previous model of the invention;

Figure 3D is a plot of transponder readings versus transponder power for the RF transponder of Figure 2, according to a previous model of the invention;

Figure 4A is a block diagram of major components of an RF transponder, according to the invention;

25 Figure 4B is a diagram of a memory space within the RF transponder of Figure 4A, illustrating how data may be arranged and transmitted, according to the invention; and

Figure 5 is a schematic diagram of a power-on reset portion of the RF transponder of Figure 4A, according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

30 As mentioned hereinabove, it is an aspect of the present invention to provide a system for monitoring vehicle tire pressure and warning the driver when a low tire inflation pressure condition occurs.

Figure 1 illustrates an RF transponder system 100 of the prior art, comprising an RF (radio frequency) transponder 102 disposed within (e.g., mounted to an inner surface of) a pneumatic tire 104. (An antenna, not shown, is mounted within the tire 104 and is connected to the transponder 102.) The transponder 102 is an electronic device, capable of transmitting an RF signal comprising unique identification (ID) information (e.g., its own serial number, or an identifying number of the object with which it is associated -in this example, the tire 104) as well as data indicative of a parameter measurement such as ambient pressure sensed by a sensor (not shown) associated with the transponder 102 to an external reader/interrogator 106. The external reader/interrogator 106 provides an RF signal for interrogating the transponder 102, and includes a wand 108 having an antenna 110, a display panel 112 for displaying information transmitted by/from the transponder 102, and controls (switches, buttons, knobs, etc.) 114 for a user to manipulate the functions of the reader/interrogator 106. Although shown as a hand-held device, the reader/interrogator may be an electronic unit mounted in a vehicle (not shown). The present invention is directed primarily to implementing an RF transponder.

As is known, the ID and/or parameter measurement information may be encoded (impressed) in a variety of ways on the signal transmitted by the transponder 102 to the reader/interrogator 106, and subsequently "de-coded" (retrieved) in the reader/interrogator 106 for display to the user. The RF transponder 102 may be "passive", in that it is powered by an RF signal generated by the external reader/interrogator 106 and emitted by the antenna 108. Alternatively, the RF transponder 102 may be "active", in that it is battery-powered. Transponder systems such as the transponder system 100 described herein are well known.

Commonly-owned, copending PCT Patent Application No. PCT/US98/07338 filed 25 14 April 1998 by Pollack, Brown, Black, and Yones (status: pending), incorporated in its entirety by reference herein, discloses a transponder, particularly a "passive" transponder which derives its operating power from an external radio frequency (RF) source, and which is associated with a pneumatic tire for use in tire identification and transmission of pressure and/or temperature data.

30 The aforementioned patent application PCT/US98/07338 discloses a transponder which is a previous model (model number "3070C") of the transponder of the present invention. Since the present invention involves commonalities with, as well as

improvements upon the previous model, relevant portions of the previous model will be described hereinbelow, with reference to Figures 2, 3, 3A, 3B and 3C.

Figure 2 is a block diagram of the model 3070C RF transponder 200 (compare 102), illustrating the major functional components thereof. This exemplary system is described as 5 an embodiment which preferably measures pressure and temperature, but it is within the scope of the invention to include measurement of other parameters which employ suitable sensors.

The transponder 200 is preferably implemented on a single integrated circuit (IC) chip shown within the dashed line 202, to which are connected a number of external 10 components. Other dashed lines in the figure indicate major functional "blocks" of the transponder 200, and include a transponder "core" 204 and a sensor interface 206. The components external to the IC chip 202 include an antenna system 210 comprising an antenna 212 and typically a capacitor 214 connected across the antenna 212 to form an L-C resonant tank circuit, an external precision resistor (Rext) 216, an external pressure-sensing 15 capacitor (C_p) 218, and an optional external maximum temperature measurement switch (MTMS) 220. The antenna 212 may be in the form of a coil antenna, a loop antenna, a dipole antenna, and the like. Alternatively, the signal output by the transponder may be provided on a transmission line. For some of these antenna embodiments (e.g., a loop 20 antenna), the capacitor 214 may be omitted since it would not be of benefit in tuning such an antenna system. In the main hereinafter, a transponder having a coil antenna is described.

The pressure-sensing capacitor C_p is preferably a rugged, low temperature coefficient, sensor with a capacitance versus pressure response having good sensitivity and linearity in the pressure range of interest. An example is an all-silicon "touch mode" capacitive pressure sensor such as are known in the art, and mentioned hereinabove.

25 The transponder core 204 includes interface circuitry 222 for processing an RF signal, such as a 125 kHz (kiloHertz) un-modulated carrier signal received by the antenna 212, for rectifying the received RF signal, and for providing voltages for powering other circuits on the IC chip 202. For example, the interface circuitry provides a regulated supply voltage (Vdd) of 2.5 volts, and a temperature-independent bandgap voltage (Vbg) of 1.32 30 volts. The provision of various supply and reference voltages for the transponder circuitry are described in greater detail hereinbelow, with reference to Figure 3B. The interface circuitry 222 also provides the received RF signal, preferably at the input frequency (F_i) it is

received, to a clock generator circuit 224 which generates clock signals in a known manner for controlling the timing of other circuits on the IC chip 202, as well as the output frequency (Fc) of a signal which is transmitted by the transponder 200 to the external reader/interrogator (e.g., 106).

5 A timing generator/sequencer circuit 226 receives the clock pulses from the clock generator circuit 224 and processes (e.g., divides) the clock pulses to generate timing windows (W_T and W_p , described hereinbelow) for predetermined periods of time (t_T and t_p , respectively) during which parameter (e.g., temperature and pressure) measurements are made. The timing windows W_T and W_p may either be of substantially equal duration or of
10 unequal duration. The timing generator/sequencer circuit 226 also controls the timing and sequence of various functions (e.g., pressure measurement and capture, temperature measurement and capture, described in greater detail hereinbelow) performed in the sensor interface 206, and is preferably implemented as an algorithmic state machine (ASM).

15 The transponder core 204 further includes a register/counter circuit 230 which includes a temperature register 232 (e.g., 12-bit) and a pressure register 234 (e.g., 12-bit) for capturing and storing temperature and pressure measurements (counts), respectively, and a block 236 of addressable memory (e.g., 120-bit), which includes an EEPROM array. The registers 232 and 234 and EEPROM array 236 are shown in a dashed line 238 representing a block of addressable memory on the IC chip 202.

20 The register/counter circuit 230 also includes a multiplexer and column decoder 240, as well as a row decoder 242 for controlling the sequence in which signals (i.e., data) are output on a line 244 to a modulation circuit 246 which, via the interface circuitry 222, communicates selected measured tire operating characteristics in a data stream via the antenna system 210 to an external reader/interrogator (e.g., 106).

25 The transponder core 204 also includes a baud rate generator 248 which controls the rate at which modulating information (e.g., the temperature or pressure measurement) is applied to the modulation circuit 246. The baud rate generator 248 also provides a data carrier clock controlling the output frequency Fc of the transponder and a data rate clock controlling a rate at which the data stream including measurements, calibration information, 30 identification, etc. is modulated onto the transponder 200 output carrier signal.

 The sensor interface 206 includes a circuit 250 for generating an output current $I(T)/N$ on a line 251 which is related to a predictable characteristic voltage of a temperature-

sensitive component (e.g., V_{be} of a transistor Q1, described hereinbelow) which is superimposed on the external resistor (R_{ext}) 216. The output current $I(T)/N$ on the line 251 is provided to a relaxation oscillator 252. In general terms, the relaxation oscillator 252 oscillates at a frequency controlled by a rate of voltage change (dV/dT) which is a function 5 of the output current $I(T)/N$ on line 251 and of internal capacitances C_{FX1} , C_{FX2} associated with the relaxation oscillator 252 as well as an external capacitance (C_p) 218 that can be switched into the oscillator circuit. An output signal $F_{osc'}$ from the relaxation oscillator 252 is provided on a line 253 which, as will be explained in greater detail hereinbelow, is indicative of both ambient temperature and ambient pressure. As used herein, the term 10 "ambient" refers to the parameter being measured in the vicinity of the transponder 200, or more particularly in the vicinity of the respective sensors associated with the transponder 200. When the transponder 200, 102 is mounted within a pneumatic tire (e.g., 104), "ambient pressure" and "ambient temperature" refer to the pressure and temperature of the inflation medium (e.g., air) within the tire 104.

15 In operation, an RF signal from an external source (i.e., reader/interrogator, not shown, compare 106) is received by the antenna 212. This RF signal is rectified and used to power the RF transponder 200. Modulating information applied to the modulation circuit 246 is used to alter characteristics of the antenna system 210 (e.g., impedance, resonant frequency, etc.). These alterations are sensed by the external reader/interrogator 106 and 20 are decoded, providing communication of temperature and pressure information back from the RF transponder 200 to the external reader/interrogator 106.

The timing generator/sequencer circuit 226 controls when the external pressure-sensing capacitance (C_p) 218 is included in the generation of a signal at frequency $F_{osc'}$ which is output by the relaxation oscillator 252, and also controls the capturing of the 25 pressure and temperature counts via the data capture circuit 254. For example, to measure temperature, the temperature-sensitive current $I(T)$ passes through the internal oscillator capacitors (C_{FX1} and C_{FX2}), but the pressure-sensing capacitor (C_p) 218 is disconnected from (not included in) those capacitances. This means that the frequency $F_{osc'}$ of the oscillator output signal seen on line 253 is a function of temperature alone. When the pressure-sensing capacitor (C_p) 218 is "switched in", then the output frequency $F_{osc'}$ of the oscillator 30 252 on the line 253 will, as explained in greater detail hereinbelow, be a function of both pressure and temperature. As described in greater detail hereinbelow, an algorithm is

employed in the reader/interrogator 106 to extract a "pressure-only" reading from the pressure-temperature measurement.

It should be noted that references made herein to "pressure readings", "pressure counts", "pressure response", "pressure register" and the like generally refer to "pressure" 5 as measured by this transponder technique which actually produces a hybrid pressure-temperature reading. When this hybrid reading has been processed to remove its temperature component, the reading will be referred to as a "pressure-only" reading.

As controlled by the timing generator/sequencer circuit 226, the data capture circuit 254 directs the relaxation oscillator output signal $F_{osc'}$ either to the temperature register 232 10 via line 255 or to the pressure register 234 via line 257, depending upon whether temperature or pressure is being measured. Counters convert the oscillator frequency $F_{osc'}$ into counts which are stored in the registers 232, 234. The timing "window" provided by the timing generator/sequencer circuit 226 has a known, controlled duration. As a result, the count remaining in (captured by) the respective temperature or pressure register (232, 15 234 respectively) when the timing window "closes" is a function of (proportional to) the oscillation frequency $F_{osc'}$ of the relaxation oscillator 252, and therefore a function of temperature or pressure, whichever is being measured during that timing window.

The EEPROM array 236 is used to hold calibration constants that the reader/interrogator (e.g., 106) uses to convert temperature and pressure counts (N_T and N_P , 20 respectively, described in greater detail hereinbelow) into temperature and pressure readings which can be displayed (e.g., via display 112) to a user. The EEPROM array 236 can also store the ID of the transponder, calibration data for the transponder, and other data particular to the given transponder.

Figure 3 is a more-detailed schematic diagram 300 of several of the components of 25 the transponder 200 of Figure 2, primarily those components described hereinabove with respect to the sensor interface section 206 of Figure 2.

In this schematic diagram 300, conventional circuit symbols are employed. For example, lines which cross over one another are not connected to one another, unless there 30 is a "dot" at their junction (cross-over), in which case the lines are connected with one another. Conventional symbols are employed for transistors, diodes, ground connections, resistors, capacitors, switches, comparators, inverters, and logic gates (e.g., "AND", "NAND", "OR", "NOR").

The circuit is described in terms of a CMOS embodiment, wherein "P" followed by a number (e.g., "P1") indicates a PMOS (P-channel) transistor and "N" followed by a number (e.g., "N1") indicates an NMOS (N-channel) transistor. CMOS transistors are of the FET (field effect transistor) type, each having three "nodes" or "terminals" - namely, a "source" (S), a "drain" (D), and a "gate" (G) controlling the flow of current between the source and the drain. In the description that follows, it will be evident that a number of the PMOS and NMOS transistors are "diode-connected", meaning that their drain (D) is connected to their gate (G). The general theory of operation of transistors, particularly CMOS transistors, is well-known to those having ordinary skill in the art to which the present invention most nearly pertains.

As will be evident from the description that follows, a number of the CMOS transistors are connected in a "current-mirroring" configuration. The concept of current-mirroring is well known, and in its simplest form comprises two similar polarity transistors (e.g., two PMOS transistors) having their gates connected with one another, and one of the pair of transistors being diode-connected. Current-mirroring generally involves causing a current to flow through the diode-connected transistor, which results in a gate voltage on the diode-connected transistor required to produce that current. Generally, the gate voltage of the diode-connected transistor is forced to become whatever voltage is necessary to produce the mirrored current through that transistor. Since the diode-connected transistor, by definition, has no gate current, by applying the gate voltage of the diode-connected transistor to any other identically-connected transistor, a mirrored-current will flow through the identically-connected transistor. Typically, the current-mirroring transistors all have the same physical area, in which case the mirrored current will be essentially the same as the current which is being mirrored. It is also known to produce a mirrored current which is either greater than or less than the current being mirrored by making one of the transistors physically larger or smaller (in area) than the other. When such identically-connected transistors having different areas are connected in a current-mirroring configuration, their scaled (larger or smaller) areas will produce correspondingly scaled (larger or smaller) currents.

In the main hereinafter, the numerous connections between the various components of the circuit are clearly illustrated in the figure, and the descriptive emphasis is on the various functions of and interactions between the various components of the circuit rather

than on reciting (ad nauseam) each and every individual connection between the various components, all of which are explicitly illustrated in the figure.

5 The antenna system 210 comprises a coil antenna 212 and an optional capacitor 214 (connected across the antenna 212 to form an L-C resonant tank circuit) providing an alternating current (AC) output to a full-wave rectifier circuit 302.

10 The full-wave rectifier circuit 302 (compare 222) comprises two PMOS transistors and two diodes, connected in a conventional manner, as shown, and outputs a full wave rectified direct current (DC) voltage on a line 303. A capacitor 304 is connected between the line 303 and ground to "smooth out" (filter) variations ("ripple") in the full wave rectified DC voltage on the line 303. The voltage on the line 303 thus becomes a usable voltage for the remaining components of the transponder - in this case, a positive supply voltage Vcc on the line 303.

15 A temperature-sensing circuit 306, corresponding approximately to the base-emitter voltage-to-current converter 250 of Figure 2, is connected between the line 303 (Vcc) and ground, and includes four CMOS transistors labeled P1, P2, N1 and N2 and a lateral bipolar transistor labeled Q1, and is connected to the external resistor 216 (Rext). The transistors P2 and N1 are diode-connected, as illustrated. The two transistors P1 and P2 are connected in a current-mirroring configuration, and the two transistors N1 and N2 are also connected in what can generally be considered to be a current-mirroring configuration. The source (S) 20 of the transistor N1 is connected via the transistor Q1 to ground, and the source of the transistor N2 is connected via the external resistor (Rext) 216 to ground.

25 As will become evident, the ability of the temperature-sensing circuit 306 to produce a signal (i.e., a current) that is proportional to a sensed ambient temperature (e.g., within the tire with which the transponder is associated) is largely dependent on the characteristic that the base-emitter voltage of the transistor Q1 is a highly predictable and repeatable function of temperature. The resistor (Rext) 216 is an external, precision, reference resistor, whose value is substantially independent of temperature (as contrasted with the temperature dependency of the transistor Q1). A suitable value for the resistor (Rext) 216 is, for example, 20.5 kilohms or 455 kilohms.

30 The transistor N2 is connected between the transistor P2 and the external resistor 216 (Rext) in a "source-follower" mode. As a voltage is impressed on the gate (G) of the transistor N2, its source voltage will "follow" its gate voltage (minus an inherent voltage

drop (Vgs) between its gate and its source).

As current flows through the transistor N1, its gate voltage will be offset by its gate-source voltage drop (Vgs) above the emitter voltage at the transistor Q1. Since the transistors N1 and N2 are essentially identical, with the same current flowing through each 5 of the two transistors N1 and N2, they will have identical gate-source voltage drops (Vgs). As a result, the voltage at the source of the transistor N2 across the external resistor 216 (Rext) will be essentially identical to the voltage at the emitter of the transistor Q1. Hence, applying Ohm's law ($E=IR$, or $I=E/R$), the current through the external resistor 216 (Rext) will equal the emitter voltage of the transistor Q1 divided by the resistance of the external 10 resistor 216 (Rext).

In normal operation, all of the current flowing through the external resistor (Rext) 216 flows through the source of the transistor N2 and, consequently, through the diode-connected transistor P2. By a current-mirroring connection, the current through the transistor P2 is replicated (mirrored) in the transistor P1. This ensures that the current 15 flowing through the transistors N1 and N2 will be the same, at all times, which further helps to ensure that the emitter voltage at the transistor Q1 and the voltage across the external resistor (Rext) 216 are identical, independent of voltage and process variations. As mentioned hereinabove, the transistors N1 and N2 are connected in what can generally be considered to be a current-mirroring configuration. However, since they are not strictly 20 identically connected, their function in the circuit 306 is principally for "matching" Q1 and Rext.

In essence, the circuit 306 ensures that the current $I(T)$ flowing through the external resistor (Rext) is predictable, and is a function of the absolute temperature (T) of the transistor Q1. As described in greater detail hereinbelow, this temperature-dependent 25 current $I(T)$ flowing through the external resistor (Rext) 216 is mirrored to a relaxation oscillator (312, described hereinbelow) to provide a signal indicative of the temperature of the transistor Q1 to the external reader (106, Figure 1). As described in greater detail hereinbelow, the output frequency F_{osc} of the relaxation oscillator 312 will be a function of the absolute temperature (T) of the transistor Q1.

30 At this point, it is useful to note that it is essentially the transistor Q1 that is being employed as the temperature-sensing element of the overall transponder circuit. The transponder circuit advantageously employs an inherent characteristic of such a transistor

implemented in CMOS technology that the base-emitter voltage of the transistor Q1 will vary by a predictable amount of -2.2 mv/°C (millivolts per degree Celsius).

It should be noted that the transponder of the present invention is described in terms of a "passive" device, relying on RF energy being supplied to it by an external source (106, 5 Figure 1) to power up its circuitry. However, it is within the scope of this invention that the transponder contains its own power supply, such as in the form of a battery. In either case, when first powering up circuitry such as described with respect to the temperature-sensing circuit 306, it is important to ensure that they "ramp up" to their normal operating state from their quiescent state in a reliable and predictable (controlled) manner. To this end, two lines 10 305 and 307 are illustrated which are connected between the temperature-sensing circuit 306 and a "startup" circuit 308.

The startup circuit 308 (also part of the base-emitter voltage-to-current converter 250 of Figure 2) is connected between the supply voltage (Vcc) on the line 303 and ground, and serves two main purposes: (i) to get current flowing in the temperature-sensing circuit 306 15 when the transponder (200) first starts up from a powered down state; and (ii) to mirror and convert the current flowing through the transistor P2 from a supply-referenced current to a ground-referenced current.

Startup is initiated by the transistor P3. The transistor P3 is fabricated to have high channel resistance so as to function in a "weak pull-up" mode. With its gate connected to 20 ground, it will always be "on", and will behave essentially like a resistor having a high resistance (e.g., > 1 mega-ohm).

Since, at startup, no current flows elsewhere in the circuit, the transistor P3 operates 25 to pull the gate of the transistor N3 towards the supply voltage (Vcc), thereby turning the transistor N3 "on", which effectively connects the grounded source of transistor N3 to its drain (D) which, in turn, grounds the gates of transistors P1, P2, and P4, and also grounds the drain of diode-connected transistor P2. This causes current to flow through the transistor P2 of the temperature-sensing circuit 306 into the drain of the transistor N3. Since the transistors P1, P2 and P4 are current-mirror connected (via the "Pbias" line 305), the current now flowing through transistor P2 will be mirrored in the transistors P1 and P4. 30 As current flows through the transistor P4 into the diode-connected transistor N5, a current-mirroring connection between the transistors N4 and N5 causes a corresponding current to flow through the transistor N4, thereby pulling the gate of transistor N3 to ground, thereby

effectively shutting "off" the flow of current through the transistor N3.

However, with current now flowing through the current-mirrored transistors P1, P2 and P4, current flowing from the transistor P1 through the diode-connected transistor N1 into the transistor Q1 forces the temperature-sensing circuit 306 to "start up" in its stable 5 operating point state (rather than its zero current state). After startup, the transistor N3 essentially "drops out" of the circuit, having performed its intended function.

The transistor N5 is connected in a current-mirroring configuration with the transistor N4 (and, as described hereinbelow, with the transistor N6). Therefore, essentially, with a current equivalent to the current through the external resistor (Rext) 216 flowing through the transistor N5, the same current flows through the transistor N4, thereby establishing a reference voltage (Nbias) on the line 309. The reference voltage (Nbias) on the line 309, as well as a supply voltage (Vdd) on a line 309', are provided to a current scaling circuit 310.

The supply voltage (Vdd) on the line 309' is provided in any suitable manner, such 15 as a multiple of a bandgap voltage (Vbg) generated in a conventional manner elsewhere on the chip, and its magnitude (e.g., 1.32 volts) should be independent of temperature, such as inherent to the silicon process which is employed in making the chip. The provision of such a stable (e.g., bandgap) voltage (e.g., Vbg) and the supply voltage (e.g., Vdd) derived therefrom is well within the purview of one having ordinary skill in the art to which the 20 present invention most nearly pertains, and is described in greater detail hereinbelow with respect to Figure 3B.

The current scaling circuit 310 (also part of the base-emitter voltage-to-current converter 250 of Figure 2) is constructed in the following exemplary manner. The sources of the transistors P5 and P6 are connected to supply voltage Vdd. The gate of a transistor 25 N6 receives the reference voltage (Nbias) on the line 309. The transistor N6 is connected in a current-mirroring configuration with the transistor N5 (as well as with the aforementioned transistor N4) and will therefore mirror the flow of current $I(T)$ through the transistors N4 and N5. Consequently, the flow of current through the diode-connected transistor P5 will mirror the flow of current through the transistors N4, N5 and N6.

30 The transistors P5 and P6 are connected in a current-mirroring configuration, but are fabricated (using conventional CMOS fabrication techniques) such that current flowing through the transistor P6 is scaled up or down by a ratio (N) of the physical area of the

transistor P5 to the physical area of the transistor P6. For example, if the transistor P6 is smaller in size than the transistor P5 (i.e., the transistor P5 is "N" times larger in area than the transistor P6), then the current flowing through the transistor P6 will be commensurately (N times) smaller than the current flowing through the transistor P5. Thus, the "scaled" 5 current flowing through the transistor P6, is labeled "I(T)/N" in the figure, and is provided on a line 311 (compare 251) to a relaxation oscillator circuit 312 (compare 252). It is well known that the ratio of the currents between the transistors P5 and P6 can readily be established by conventional circuit processing techniques, such as by simply making one of the transistors larger than the other, or by implementing a one of the two transistors as the 10 aggregate of two or more same-size transistors so that their aggregate area is larger than the area of the other of the two transistors.

The relaxation oscillator circuit 312 (compare 252) is of fairly conventional design, and includes a measurement switching circuit 315 at the "front end" of a set-reset circuit 314 comprising two phase paths 314a, 314b. This circuit 315 comprises a pair of 15 complementary transistors P7 and N7 connected to a charged side of a measurement capacitor C_{FX1} at the front end of a one phase path ($\phi 1$) 314a; and another pair of complementary transistors P8 and N8 connected to a charged side of another measurement capacitor C_{FX2} , plus a switch 350 to add another measurement capacitor C_p , all at the front end of another phase path ($\phi 2$) 314b.

Connected as illustrated, for a given pair of transistors (e.g., P7 and N7), when their common gate voltage is high (i.e., towards positive supply) their output (e.g., to phase path 314a) will be grounded (connected to ground and isolated from current $I(T)/N$ on line 311), and when their common gate voltage is low, their output will provide the current $I(T)/N$ flowing on the line 311 to a respective one of the phase paths (e.g., 314a) of the relaxation 20 oscillator 312. As is known for circuitry such as the relaxation oscillator 312, when the common gate voltage of a one of the pairs of transistors (e.g., P7 and N7) is high, the common gate voltage of the other of the pairs of transistors (e.g., P8 and N8) will be low, and vice-versa. In this manner, each phase path 314a and 314b has a duty cycle (i.e., its 25 "on" time), which may be the same as or may be different than the duty cycle of the other phase path 314b and 314a, respectively. Thus, each pair of transistors (e.g., P7 and N7) may be considered to be an "input switch" to its respective phase path (e.g., 314a).

Each phase path 314a and 314b of the relaxation oscillator 312 has a comparator

316a and 316b, respectively, at its input, and has a fixed-value capacitor C_{FX1} and C_{FX2} , respectively, connected between the negative (-) input of the comparators 316a and 316b and ground. The capacitors C_{FX1} and C_{FX2} have exemplary capacitance values of 2-5 pf (picofarads) and 2-5 pf, respectively, and are preferably implemented as equal-valued "on-chip" devices, such as poly-to-poly capacitors exhibiting a low temperature coefficient (e.g., less than 20ppm). The positive (+) inputs (terminals) of the comparators 316a and 316b are tied together and are set to a reference threshold voltage V_{bg} , such as 1.32 volts, which is independent of temperature.

5 A "NOR" logic gate 318a and 318b is connected at the output of each phase path 10 314a and 314b, respectively, and the two NOR gates 318a and 318b are cross-connected to form a latching circuit having an output on a line 319a and 319b. The cross-connected NOR gates 318a and 318b are thus capable of functioning as a flip flop, or an RS (re-set/set) latch.

15 When the common gate voltage of one of the input switches (e.g., P7 and N7) is high, the respective capacitor (e.g., C_{FX1}) for that phase path (e.g., 314a) is grounded (shorted out, caused to be devoid of charge). Conversely, when the common gate voltage of one of the input switches (e.g., P7 and N7) is low, the scaled current $I(T)/N$ from line 311 is applied to (allowed to flow into) the respective capacitor (e.g., C_{FX1}) for that phase path (e.g., 314a), and the capacitor begins to charge (acquire an increasing voltage across the capacitor). When the voltage across the capacitor C_{FX1}/C_{FX2} reaches the comparator 20 reference voltage V_{bg} the output of the comparator 316a/316b goes low and changes the state of the output of the latch 318a/318b on the line 319a/319b. In this manner, the relaxation oscillator 312 will oscillate at a frequency F_{osc} determined by the rise time of the capacitors C_{FX1} and C_{FX2} and, importantly, by the scaled current $I(T)/N$ being supplied to the capacitors C_{FX1} and C_{FX2} . With greater current $I(T)/N$ being supplied, the voltages of the capacitors C_{FX1} and C_{FX2} will rise faster, crossing the threshold voltage faster, and causing 25 the relaxation oscillator 312 to oscillate faster, thereby increasing the frequency F_{osc} of the signal on the line 319a. The signal on the line 319a is inverted by an inverter 320, as shown, to provide a signal of frequency F_{osc}' on the line 321.

30 As described in greater detail hereinbelow, the oscillator 312 is controlled to run in two mutually-exclusive modes, a temperature-sensing mode (between times t_0 and t_1) and a pressure-sensing mode (between times t_1 and t_2), as controlled by the timing generator/sequencer 226. The frequency of the oscillator output signal F_{osc} (and F_{osc}')

will be different in each of these two modes.

GENERATING TEMPERATURE AND PRESSURE READINGS

In the exemplary context of the transponder 200 being associated with a pneumatic tire, it is principally desirable to determine the pressure within the pneumatic tire. For 5 example, a typical passenger vehicle tire may be properly inflated at about 32 psi (about 221 kPa). Since tire inflation pressures are normally specified as "cold" pressures (pressure measured when the tire is not heated by operation), and since a monitoring device will be reporting pressures measured in tires which are most likely in use and therefore "hot", it is secondarily desirable to determine the temperature of the inflation medium (e.g., air) within 10 the pneumatic tire. Utilizing the temperature measurement, a monitoring system (e.g., 106) can, for example, convert the measured pressure to a "cold" pressure with simple calculations based on the ideal gas law ($PV = \mu RT$). This "cold" pressure could be considered a "temperature-independent" pressure, which is also an indication of the mass of 15 air contained by the tire. With reference to the transponder 200, the hybrid "pressure" measurement it produces must be converted (by different calculations detailed hereinbelow) to a true pressure-only measurement before it can be used in such gas-law calculations.

It is, for example, estimated that an approximate 10% decrease in fuel consumption could be realized if the pneumatic tires on vehicles were operated at their specified pressure. Although vehicle fleet operators are typically sensitive to this issue, and check and adjust 20 tire pressure frequently, the average operator of a passenger vehicle is often less inclined to keep an eye on their tire pressure until, for example, the tire is visibly flattened out. In such cases, an LCD (liquid crystal display) readout or the like on the dashboard of a car could provide dynamic tire inflation information to the operator of a vehicle, the pneumatic tires of which are equipped with a transponder such as the one described herein. Of no less 25 significance is the emergence of "run-flat" tires being marketed by various tire manufacturers. The Goodyear EMT (extended mobility technology) series of tires is an example of a "run-flat" tire, an overall purpose of which is to allow a driver to travel up to 50 miles (approximately 120 kilometers) on a deflated ("flat") tire, at "reasonable" operating speeds (e.g., 60 miles per hour, or 144 kilometers per hour), while maintaining 30 normal control over the vehicle. Such run-flat tires are generally well known, and do not form a portion of the present invention, per se. When running "flat" on a run-flat tire, it is particularly important that the driver be alerted to the fact that he or she is operating the

vehicle on "borrowed time" as indicated, principally, by an indication, whether visual or audio (e.g., a beep) that the tire is indeed "flat" and needs to be repaired or replaced at his or her earliest convenience (and before the run-flat mileage limit).

By allowing the relaxation oscillator 312 to run, the frequency of its output signal 5 Fosc (and Fosc') will be a function of the absolute temperature of (sensed by) the transistor Q1. This is true in both the temperature-sensing mode and the pressure-sensing mode of operation.

In the temperature-sensing mode, and in the case that the capacitance values for C_{FX1} 10 and C_{FX2} are equal, which is preferred, the relaxation oscillator 312 will have a symmetrical (balanced, 50%) duty cycle. In the pressure-sensing mode, the pressure-sensing capacitor (C_P) 218 is switched by a semiconductor switch 350 across C_{FX2} , which changes the duty cycle and output frequency Fosc (and Fosc') of the relaxation oscillator 312.

In the temperature-sensing mode, only the fixed capacitors C_{FX1} and C_{FX2} are being alternately charged (and discharged) resulting in a 50% duty cycle with a period 15 proportional to ambient temperature. In the pressure-sensing mode, the pressure-sensing capacitor (C_P) 218 is switched into phase path 314b of the oscillator 312. Thus, for a given temperature, for the first half of the oscillator period the phase path 314a behaves in the same manner as in the temperature-sensing mode, and for the second half of the oscillator period the phase path 314b behaves in a manner that is proportional to the capacitance value 20 of the fixed capacitor C_{FX2} plus the capacitance value of the pressure-sensing capacitor (C_P) 218. This, in effect, slows down the oscillator and changes its duty cycle. The change in the duty cycle is indicative of the ratio of C_P to C_{FX2} . Thus, from the ratio of the two periods (with and without C_P in the circuit, it is straightforward to calculate what the additional capacitance C_P is, hence the sensed pressure. As described in greater detail 25 hereinbelow, the temperature-dependency of the oscillator output in the pressure-sensing mode can be completely eliminated, in a straightforward manner.

The "slowing down" of the oscillator when the pressure-sensing capacitor (C_P) 218 is switched into the oscillator circuit results, inevitably, in there being relatively fewer oscillator output pulses (reduced output frequency) to count during a given pressure-measurement window (e.g., W_P) than during a similar duration temperature-measurement window (e.g., W_T). In other words, a "slowed-down" oscillator will reduce that rate at which counts indicative of the parameter measurement are collected. In order to increase

the resolution (quantity) of the counts (N_p) generated during the pressure-measurement window (W_p), it is contemplated that the pressure-measurement window (W_p) can be increased in size (changed in duration) so as to allow for the capture of an appropriate number of pressure counts in the pressure register 234. This can readily be accomplished 5 simply by establishing a larger (than otherwise) value for the time t_2 which establishes the end of the pressure-measurement window (W_p) in the pressure-sensing mode (between times t_1 and t_2), as controlled by the timing generator/sequencer 226. For example, the temperature-measurement window W_T (between times t_0 and t_1) can be on the order of several ones (e.g., eight) of milliseconds, and the pressure-measurement window W_p can be 10 on the order of tens or dozens (e.g., eighty) of milliseconds. Alternatively, it is contemplated that the scaled current ($I(T)/N$) flowing out of the current scaling circuit 310 to the relaxation oscillator 312 could be increased during the pressure-measurement window (W_p) to increase the fundamental frequency of the relaxation oscillator 312, thereby increasing the overall resolution of the pressure count. This can readily be accomplished, 15 for example in the case of transistor P6 being smaller in size (area) than the transistor P5, simply by switching in a transistor P6' (not shown) in lieu of the transistor P6, the transistor P6' having a larger area than the transistor P6 so that the ratio of the areas of the transistors P5 and P6 is closer to unity (i.e., less scaled down) and the current to the relaxation oscillator 312, hence its counting rate, is increased. Such switching in of another transistor 20 P6' is readily effected with a switch (not shown) comparable to the aforementioned switch 350 which switches in the pressure-sensing capacitor (C_p) 218. One having ordinary skill in the art to which the present invention most nearly pertains will readily understand how to offset the "slowing down" of the oscillator when the pressure-sensing capacitor (C_p) 218 is switched into the oscillator circuit, in light of the teachings presented herein.

25 OPTIMIZING PRESSURE-RESPONSIVENESS

Obtaining (and displaying) an accurate pressure reading being of paramount importance when monitoring the pressure of a pneumatic tire, certain parameters of the transponder circuit may be established to maximize its pressure-responsiveness and therefore improve the accuracy of the pressure reading displayed by the external reader/interrogator 30 (e.g., 106).

As described hereinabove, the transponder responds to the changing capacitance of the pressure sensor (C_p) 218 by changing the value of a binary 12-bit word that is

transmitted to the external reader/interrogator 106. This binary word is the count of an oscillator frequency during a timing window W_p (between t_1 and t_2) established by the timing generator/sequencer 226. The pressure response can therefore be described as the change in counts per unit change in capacitance of the pressure-sensing capacitor (C_p) 218.

5 Pressure-responsiveness (and resolution) of the transponder has been found to be dependent on a number of factors, each of which can be analyzed. For example, it has been determined that:

- (a) Increasing the pressure-measurement window W_p to make it larger than the temperature-measurement window W_t will increase the pressure count N_p (and not the temperature count N_T) for a given value of the pressure-sensing capacitor (C_p) 218, to make up for the relatively lower oscillator frequency which occurs during pressure measurement compared to temperature measurement (as detailed hereinabove).
- (b) Increasing the scaled current $I(T)/N$ to the oscillator 312 will proportionally increase the pressure count N_p for a given value of the pressure-sensing capacitor (C_p) 218.
- 10 (c) Decreasing the values for capacitor(s) C_{FX1} and/or C_{FX2} will proportionally increase the pressure count N_p for a given value of the pressure-sensing capacitor (C_p) 218.
- (d) Increasing the scaled current $I(T)/N$ to the oscillator will proportionally increase the pressure count N_p (for a given value of C_p) at a greater rate than decreasing the values for capacitors C_{FX1} and C_{FX2} .
- 15 (e) Increasing the scaled current $I(T)/N$ will increase both the pressure counts N_p and the temperature counts N_T unless the current increase can be made to occur only during the pressure-measurement window W_p .
- (f) Decreasing the values for capacitor(s) C_{FX1} and/or C_{FX2} will increase both the pressure counts N_p and the temperature counts N_T even if only one of the capacitors is changed.

20 As a general proposition, increasing the pressure counts N_p is desirable. However, one having ordinary skill in the art to which the present invention most nearly pertains will readily appreciate that there is a practical upper limit to increasing the pressure counts at a frequency which may become unacceptably large for the capability of certain circuits of the IC chip.

MEASURING PARAMETERS

30 Figure 3A illustrates the components involved in the final step of capturing

temperature and pressure measurements in the transponder. The signal F_{osc}' output by the relaxation oscillator 312 is provided on line 321 (compare 253) to an input of each of two AND gates 360 and 362 in the data capture circuit 254. A signal ("Capture Temp") is provided by the timing generator/sequencer 226 to the other input of the AND gate 360 5 during the temperature-sensing window (W_T) so as to load the temperature register 232 via line 255 with the count ("data," or "reading") N_T indicative of measured temperature. Another data signal ("Capture Press") is provided by the timing generator/sequencer 226 to the other input of the AND gate 362 during the pressure-sensing window (W_P) so as to load 10 the pressure register 234 with the count ("data," or "reading") N_P indicative of measured pressure. Each of the registers 232, 234 has a counter (not shown) associated with it to convert the incoming oscillating signal F_{osc}' to a stored count. The two counts N_T , N_P are then shifted out of the registers 232 and 234, via the MUX 240, to the modulation circuit 246 described hereinabove.

When the transponder is powered up, temperature and pressure are continuously 15 measured, and these measurements are transmitted back to the external reader/interrogator 106 as data words in a data stream. For example, each of the temperature and pressure parameters can be transmitted back to the reader/interrogator 106 as 12-bit data words in selected (known) portions of a larger (e.g., 144-bit) data stream. One bit in the overall data stream may be dedicated to the state (e.g., "closed" or "open") of the MTMS switch 220. A 20 complete description of an exemplary data stream being transmitted by the transponder to the external reader/interrogator is set forth hereinbelow with reference to Figure 3C.

Temperature is suitably measured by counting the number of cycles output from the oscillator 312 during a fixed time period (window W_T of time from t_0 to t_1) having a time 25 period t_T . For example, a down-counter (not shown, but associated with the temperature register 232) may be clocked by the oscillator, such that at the end of the window W_T time period t_T , a temperature count N_T is generated. The relationship between temperature count N_T and temperature is substantially linear for the circuitry 300 of this embodiment.

Similarly, pressure can be measured by counting the number of cycles output from 30 the oscillator 312 during a fixed time period (window W_P of time from t_1 to t_2) having a time period t_P . For example, a down-counter (not shown, but associated with the pressure register 234) may be clocked by the oscillator, such that at the end of the window W_P time period t_P , a pressure count N_P is generated. The relationship between pressure count N_P

and pressure is a predictable function of both actual pressure and temperature for the circuitry 300 of this embodiment. As explained hereinbelow, by manipulating the temperature and "pressure" counts (N_T and N_p) this hybrid pressure-temperature value can be used to determine a pressure-only value.

5 **OBTAINING A PRESSURE-ONLY READING AT THE
READER/INTERROGATOR**

The fundamental frequency of the oscillator 312 is set by parameters in the IC chip (e.g., 202) and, as described hereinabove, is temperature-dependent. Therefore, the pressure response N_p is a function (hybrid) of both temperature and pressure, and the 10 relationship of N_p to C_p is nonlinear. Therefore, using a linear equation for calculating the pressure response would inevitably lead to significant errors over a range of pressures being measured. However, for limited ranges of pressures being measured, for example over a 20 psi (138 kPa) range of pressures, using a linear equation may be acceptable. A better approximation might be obtained using a polynomial equation, but this would complicate the 15 reader/interrogator logic, making for slower response, and would require additional calibration constants.

An important advantage of using the transponder circuitry described hereinabove is that the relationship of N_T/N_p to pressure sensor capacitance C_p is linear, and requires no 20 temperature compensation term in the equation (algorithm) used by the reader/interrogator 106 to calculate pressure, thereby greatly simplifying the design of the reader/interrogator. (This also assumes the use of a pressure sensor (C_p) 218 which has a substantially linear relationship between pressure and capacitance.) This beneficial "ratiometric" relationship is readily demonstrated by the following equations:

Generally,

25 $\text{count} = \text{counting window time (t)} * \text{frequency (F)}$

$$F = 1/\text{period}$$

$$\text{Charging time} = V * C / I$$

for a capacitor with capacitance C to be charged to a voltage V with a current I .

Since the period of the relaxation oscillator 312 with output signal of frequency 30 F_{osc} is the sum of the charging times for the capacitances in the two phase paths 314a and 314b, the above equations can be manipulated to obtain a general equation for the count from such a relaxation oscillator with capacitances C_{FX1} and C_{FX2} , for example:

$$\text{count} = t/(V^*C_{FX1}/I + V^*C_{FX2}/I) = t^*I/(V^*(C_{FX1} + C_{FX2}))$$

Substituting the values for the temperature and pressure counts:

$$N_T = (t_T^*I(T)/n_T)/(Vbg^*(C_{FX1} + C_{FX2})) \quad [\text{EQ. A}]$$

$$N_P = (t_P^*I(T)/n_P)/(Vbg^*(C_{FX1} + C_{FX2} + C_P))$$

5 where n_T and n_P are values for the scaling factor N in the scaled current

$I(T)/N$ which could be different during the temperature and pressure measurement windows, respectively.

Dividing equations to obtain N_T/N_P :

$$N_T/N_P = (t_T/t_P)*(n_P/n_T) * (C_{FX1} + C_{FX2} + C_P)/(C_{FX1} + C_{FX2})$$

10 or

$$N_T/N_P = (t_T/t_P)*(n_P/n_T) * (1 + (C_P/(C_{FX1} + C_{FX2}))) \quad [\text{EQ. B}]$$

Since everything to the right of the equals sign is a defined constant except for the pressure-sensing capacitance C_P , it can be seen that there is a linear relationship between N_T/N_P and C_P (and thus pressure). This means that N_T/N_P is only a function of pressure, and is 15 insensitive to temperature or capacitor-charging current variations.

If none of the response optimization steps described hereinabove have been utilized, then the equation EQ. B can be simplified since capacitors C_{FX1} and C_{FX2} have the same value C_{FX} ; the measurement windows W_T and W_P have the same time width $t_T = t_P = t_w$ (e.g., 8.192 ms); and the current scaling factors n_T and n_P have the same value N :

$$20 \quad N_T/N_P = 1 + (C_P/2*C_{FX})$$

It can be seen from equation EQ. A that there is already a linear relationship between the temperature count N_T and the current $I(T)$ (which is, in turn, proportional to temperature).

In both of the measurement equations EQ. A and EQ. B it can be seen that linear 25 relationships exist, but the slope and intercept of these equations are complex combinations of multiple parameters which are unique to a given transponder design, and are likely to be different even for each transponder of a given design due to manufacturing variances. In a simple embodiment of this invention, the transponder could transmit only the counts N_T and N_P to a reader/interrogator, and the reader/interrogator would have to use assumed average 30 values for slope and intercept in order to determine temperature and pressure. This could cause significant inaccuracy, so the preferred embodiment as described herein stores calibration constants in the transponder memory (e.g., 236) and transmits these calibration

constants with the measurement counts N_T and N_p , so that the reader/interrogator (e.g., 106) can accurately calculate temperature and pressure using linear equations customized/optimized for the individual transponder generating the measurements. The linear equations used in the exemplary reader/interrogator (e.g., 106) are of a well-known "point-slope" form:

$$y - y_1 = m(x - x_1)$$

where:

(x_1, y_1) is the defining point; and

m is the slope.

10 The slope (m) can be determined from any two points on the line: (x_1, y_1) , (x_2, y_2) :

$$m = (y_2 - y_1) / (x_2 - x_1)$$

Substituting for x and y , a specific equation for the temperature response line becomes:

$$N_T - N_{T1} = m_T(T - T_1)$$

Choosing a value such as 25°C for temperature T_1 yields the equation:

$$15 N_T - N_{T25} = m_T(T - 25)$$

Solving for N_T yields the following equation for the temperature response line:

$$N_T = m_T(T - 25) + N_{T25}$$

wherein the slope m_T of the temperature response line is:

$$m_T = (N_{T2} - N_{T1}) / (T_2 - T_1)$$

20 As long as the reader/interrogator "knows" the assumed defining point temperature (e.g., 25°C), then it will be able to calculate a temperature (T) from a received value of temperature count N_T using the calibration constants: a defining point temperature count N_{T25} and a slope m_T which are also transmitted to the reader/interrogator. A similar set of equations can be applied to determine pressure from transmitted pressure (and temperature) counts and pressure calibration constants. As noted hereinabove, the pressure-only reading is best determined from a linear equation utilizing a ratio N_T/N_p (temperature count divided by pressure count) instead of just the pressure count N_p .

25 The calibration constants are determined in a calibration process which includes exposing each transponder to a set of controlled, known temperature and pressure conditions and recording the corresponding set of temperature and pressure counts (N_T and N_p) generated by that transponder. Calculations on these calibration test results determine four calibration constants which are then stored in the transponder memory (e.g., 236). The four

calibration constants are numbers representative of the slope and defining point for a linear response of temperature versus temperature count N_T , and pressure (only) versus count ratio N_T/N_P .

GENERATING RELIABLE SUPPLY AND REFERENCE VOLTAGES

5 As described hereinabove, the positive (+) inputs (terminals) of the comparators 316a and 316b are tied together and are set to a reference "bandgap" voltage V_{bg} , such as 1.32 volts, which is independent of temperature. As also mentioned hereinabove, the supply voltage (Vdd) on the line 309' may be provided as a multiple of the reference bandgap voltage (V_{bg}) so as to be a stable operating voltage for the current scaling circuit 310 and 10 the relaxation oscillator 312.

15 Figure 3B illustrates a circuit 370 suitable for generating the supply voltage Vdd. A temperature-independent calculable bandgap voltage V_{bg} is readily derived, based on the processing techniques employed in fabricating the IC chip, as being inherent to the selected process (e.g., CMOS). This bandgap voltage V_{bg} is provided to the positive (+) input of an operational amplifier 372, connected as shown, in a feedback loop having gain, to 15 provide supply voltage Vdd as an integral multiple of the bandgap voltage V_{bg} .

AN EXEMPLARY DATA STREAM

20 As mentioned hereinabove, information (data) from the transponder is transmitted to the external reader/interrogator in the form of a data stream, a portion of which is the temperature count N_T , another portion of which is the pressure count N_P , and another portion of which represents the state (e.g., "closed" or "open") of the MTMS switch (220). Remaining portions of the data stream may contain information which is personalized to a 25 given transponder unit such as its ID information (e.g., serial number), calibration constants, and the like.

25 Figure 3C illustrates an exemplary architecture for information which is stored in memory (e.g., 238) within the transponder 200, as well as a data stream which is transmitted by the transponder 200 to the external reader/interrogator 106. The memory 238 of the transponder core 204 has, for example, a 144-bit address space which includes 119 (one hundred nineteen) bits of programmable memory and one address location 30 dedicated to the state of the MTMS switch 220 - these 120 (one hundred twenty) bits of programmable memory constituting the EEPROM 136 - plus two 12-bit temperature and pressure registers 232 and 234, respectively.

Each of the 119 programmable memory bits can separately be written to with any combination of data, including synchronization (sync) pattern information, general data, error checking codes, and temperature and pressure calibration data. The EEPROM is 'block writeable', meaning that in the 'write' mode, the entire 120 bits of EEPROM are 5 programmed to a logical (binary) value of "1". Individual bits can be 'erased' (set to a logical value of "0" simply by clocking the chip to the bit's physical address and placing the chip into the 'erase' mode). The address location is preserved.

In this example, the first twelve data locations (000..011 in ROW 1) are reserved for sync. The next seventy one data locations (012..082 in ROWs 2 through 7) are for general 10 information and a value for a data validation algorithm such as CRC (Cyclic Redundancy Check). The next data location (083) contains the logic level (state) of the MTMS switch 220. A logical value of "1" indicates that the MTMS switch is open and a logical value of "0" indicates that the MTMS switch is closed.

As mentioned hereinabove, each transponder unit is suitably calibrated prior to its 15 installation in a tire. The next twelve data locations (084..095 in ROW 8) hold temperature calibration (e.g., defining point) data ("TEMP COMP"). The next twelve data locations (096..107 in ROW 9) hold pressure calibration (e.g., defining point) data ("PRESS COMP"). The next twelve data locations (108..113 and 114..119 in ROW 10) hold calibration (e.g., slope) information for temperature and pressure, respectively.

20 As counts N_T and N_p for temperature and pressure are generated, as described hereinabove, they are stored in ROWs 11 and 12 of the overall memory space, which correspond to the temperature and pressure registers 232 and 234, respectively. Various predetermined values can be stored to indicate error conditions such as overflow and short-circuit.

25 OPERATING FREQUENCIES AND MODULATION

The transponder of the present invention is not limited to any particular operating frequency. The choice of operating frequency will depend largely upon factors such as where the transponder is mounted in relationship to the object it is monitoring, the location 30 of the reader/interrogator antenna (108), and relevant government regulations permitting (conversely, restricting) data transmissions of the type set forth herein in selected portions of the overall RF frequency spectrum.

An example of suitable operating frequencies for operating the transponder in the

United States is 60 KHz to 490 KHz.

The transponder can be polled (and powered) by the reader/interrogator 106 at a first "interrogation" frequency (F_i), and the data stream can be transmitted back to the reader/interrogator at a second "data carrier" frequency (F_c) which is, conveniently, a whole number multiple or fraction of the interrogating frequency. For example, $F_c = F_i/2$. Or, 5 $F_c = F_i/4$. The frequency (F_c) at which the data stream is transmitted back to the reader/interrogator is independent of the data rate, which is established by the clock generator 224 and the baud rate generator 248. However, one having ordinary skill in the art to which the present invention most nearly pertains will recognize that the range of 10 available baud rates will typically be significantly less than the interrogation frequency (F_i). The baud rate is preferably derived from the interrogation frequency (F_i) of the reader/interrogator, such as a whole number fraction thereof. For example, the baud rate may be set at $F_i/32$ (or, in the case of $F_c = F_i/2$, the baud rate can be set to $F_c/16$).

For example, the interrogation frequency (F_i) may be 125 KHz, and the data carrier 15 (F_c) may be set to 62.5 KHz, or half of the interrogation frequency.

In another example, an interrogation frequency (F_i) of 13.56 MHz has been found to be suitable.

The data stream, such as the exemplary data stream described with respect to Figure 20 3C is impressed by the modulator circuit 246 onto the antenna 212, and transmitted to the reader/interrogator 106. It is within the scope of this invention that any suitable modulation scheme be employed, including amplitude modulation (AM), frequency modulation (FM), frequency shift keying (FSK), and phase shift keying (PSK). However, phase shift keyed 25 (PSK) is preferred. AM modulation is not particularly well-suited to digital transmission. Frequency modulation schemes such as FM or FSK may be somewhat problematic with regard to propagating the data-modulated transponder output signal through the medium of a pneumatic tire (e.g., 104).

RATIO VERSUS SIGNAL STRENGTH

An added advantage of using the ratio N_T/N_p for a pressure indicator accrues because 30 it has been determined that the ratioed value is less sensitive to variations in coupling between the reader/interrogator and the transponder than either of the N_T and N_p measurements taken alone. This is illustrated in Figure 3D which shows a graph 390 of measurement counts (on vertical axis 394) versus power (on horizontal axis 392). For a

passive transponder 200 such as described in the preferred embodiment of this invention, the transponder power is supplied by the RF signal from the reader/interrogator (e.g., 106). If the RF coupling strength weakens due to transmission or reception problems including excessive distance or interference, then the power in the transponder 200 circuitry may 5 decrease. It has been determined that for power levels below a certain value PWR_1 , the relaxation oscillator 312 outputs a lower than normal frequency signal $Fosc'$ and thus reduces the temperature and pressure counts N_T and N_P below what they should be for a given temperature or pressure. The effect is illustrated by the downward curve on the plot 396 of temperature count N_T and on the plot 398 of pressure count N_P as the plots extend 10 below the minimum power PWR_1 . Fortunately, the low-power effect is proportionally the same for both counts, so that the ratio N_T/N_P (plot 399) becomes relatively steady for all power levels down to a minimum power PWR_0 needed to operate the transponder 200. Thus, by determining (during calibration) and storing calibration data for the ratioed value 15 of N_T/N_P in the transponder, the ability to determine a pressure-only reading which is relatively insensitive to coupling variations between the reader/interrogator and the transponder is both simplified and made more reliable.

IMPROVEMENTS, GENERALLY

The present invention deals with a new "RFIQ™" transponder 400 (see Figure 4A) which implements improvements to the previous model, "3070C" transponder 200 described hereinabove. A number of improvements have been made, and new features incorporated, including, but not limited to:

- Lower power consumption.
- Increased oscillator stability vs. Power or Frequency.
- Increased resolution of temperature and pressure counts.
- Increased electrostatic discharge (ESD) protection to more than 2200V.
- Increased, programmable modulation index (magnitude of PSK modulation applied to the RF signal).
- Reduced number of external connection pins for programming and testing.
- Increased Digital and Analog Testability.
- Increased to 192 bits of data stream.
- Increased to 156 bits of programmable EEPROM.
- Programmable with the antenna (coil) attached.

- 6 bits of parity – 1 bit for each 4 bits of NT, NP data.
- Programmably scale currents to independently optimize reading counts for pressure and temperature.
- 3V Battery powered mode for use in “active” implementations of the transponder (“active tags”).
- 5 • Power-On Reset.
- Base-band data output on a test pin.

PROBLEMS TO BE SOLVED

10 In particular, there are general problems with the previous transponder design 200 described hereinabove. It is believed that improvements which are the subject of the present invention provide solutions for a number of these problems:

- The relaxation oscillator of the previous design transponder 200 could be adjusted to optimize the pressure and temperature counts (NP and NT) for a desired pressure and temperature range, but the adjustment could only be accomplished during integrated circuit production. It is desirable to provide a way to optimize the counts NP and NT after integrated circuit production.
- When the previous design transponder 200 is used (as a passive transponder), inaccurate results may be transmitted when the transponder operates at too low a power input, such as during startup, or when distant from the reader/interrogator. (For example, refer to Figure 3D.) In addition, the previous model would start modulating (“transmitting”) as soon as it received an interrogation signal of any strength, and would start the transmission at a random location in the data word. If the initial signal was weak (from a distant reader/interrogator), then the voltage supplies could be insufficient to produce valid temperature and pressure readings. And if modulation started before sufficient power levels were developed, then the power drain of signal modulation would aggravate the insufficient power problems. A further problem occurs if the relaxation oscillator does not start each measurement cycle in a consistent, defined state.
- The previous design transponder 200 has a fixed modulation index (magnitude of RF signal modulation) which is determined during integrated circuit production. It is desirable to provide a way to optimize the transponder for different combinations of antenna (“coil”) 210 and reader/interrogator 106, and for different operating conditions. Also, certain transponder applications utilize an external zener clamp across the antenna

210 for better stability, but the zener can cause the previous design transponder 200 to be "read-limited".

5 • Although the previous design transponder 200 can have certain operating characteristics adjusted ("trimmed") during manufacture (e.g., current scaling via size adjustments to transistors), these manufacturing changes are permanent, and not easy to vary from transponder to transponder. Furthermore, if trim settings were to be implemented in programmable memory (e.g., EEPROM), then there would be other problems with accessing those settings during power-up, and continuously rather than through row (242) and column (240) decoders.

10 Other improvements and problem solutions may become evident in the description to follow.

GENERAL DESCRIPTION

15 The improved RFIQ™ transponder 400 (compare 200, 102) is a custom CMOS, low voltage Integrated Circuit ("IC", or "chip") that can measure temperature and pressure as a low-frequency "passive" (RF signal-powered) transponder or as an "active" (battery-powered) measurement system. The IC provides programmable trimming that determines: (a) if the part is active or passive, (b) to adjust temperature and pressure resolution, and (c) modulation index and coil clamping strength (when in the passive mode).

20 In the passive mode, the IC develops power from a reader/interrogator RF signal that is coupled to an external LC circuit across the transponder antenna inputs. The transponder uses the signal received to provide power and to generate an on-chip clock. The transponder sends back its memory contents to the reader by modulating the impedance of the antenna, which is known as "back scattered modulation". The reader demodulates the returned data to get the sensor identification ("ID") as well as sensor data and calibration constants needed to interpret the data.

25 The transponder sends a 196-bit serial phase-shift-keyed (PSK) data-stream as sixteen, 12-bit words. The first 12 bits are the programmable sync word, with each sync bit being 1.5 bits wide. Next, 144 bits of EEPROM are transmitted that are of normal bit width. The 144 bits contain the unique ID code of the transponder, the calibration constants for temperature and pressure data, and a CRC for error checking. The transponder then sends 36 bits of data: a 12-bit temperature count (NT), a 12-bit pressure count (NP), and a 12-bit word consisting of five unused bits as 1's, 1 bit for the state of the MTMS over-temperature

sensor, and 6 bits of even-parity, with one bit of parity for every four bits of NP and NT data.

In the active mode, the transponder must be controlled by external hardware. The controlling hardware provides power to the IC and a clock signal via either the CLK or VB pads. The IC shifts out its data on the DATA pad on every falling edge of the clock. The 5 clocks must be given at a precise clock rate so that temperature and pressure are collected during fixed periods of time and therefore, the hardware can optimize the clocking time per bit to get the highest resolution for temperature and pressure. The IC can operate down to as low as 2.8V in active mode.

10 As either a passive or active tag (transponder), the IC can be tested after assembly by applying power and talking to the chip via a 4-pin interface. This interface allows the user access to the chip's EEPROM and allows testing the chip functions. The EEPROM data can be read, cleared, or programmed and the oscillator tested by directly reading the frequency. The chip sensor oscillator can also be tested and provides a second method for reading 15 temperature and pressure in the active mode.

OVERVIEW OF THE RFIQ™ TRANSPONDER CIRCUITRY

Figure 4A is comparable to Figure 2, and is a block diagram of a relevant portion of an improved RFIQ™ transponder 400 (compare 102, 200), illustrating the following signals, 20 terminals and functional blocks (sections), and their interconnections with one another. This exemplary system is described as an embodiment which preferably measures pressure and temperature, but it is within the scope of the invention to include measurement of other parameters which employ suitable sensors.

The transponder 400 is preferably implemented on a single integrated circuit (IC) chip shown within the dashed line 402 (compare 202), to which are connected a number of 25 external components. Other dashed lines in the figure indicate major functional "blocks" ("sections") of the transponder 400, and include a block 438 (compare 238) of addressable memory, and a sensor interface section 406 (compare 206).

The components external to the IC chip 402 include an antenna system 410 (compare 30 210) comprising an antenna (coil) 412 and an optional capacitor 414 connected across the coil 412 to form an L-C resonant tank circuit, an external precision resistor (Rext) 416 (compare 216), an external pressure-sensing capacitor (C_p) 418 (compare 218), and an optional external maximum temperature measurement switch (MTMS) 420 (compare 220).

Each external component has an appropriately labeled connection pad as shown in Figure 4A: VA and VB for the antenna system 410; Rext, Cp and MTMS for the high side of the precision resistor 416, the pressure-sensing capacitor 418, and the maximum temperature measurement switch 420, respectively. The ground connection for the analog external components Rext, Cp, and MTMS should be made via the analog ground AGND pad. The other ground pad (GND) is for the ground connection of external digital connections. The remaining connection pads are for use in active or test modes of transponder 400 operation as described hereinbelow.

The antenna 412 may be in the form of a coil antenna, a loop antenna, a dipole antenna, and the like. It is mainly used when the transponder 400 is in the passive mode. Alternatively, when the transponder 400 is in the active mode, the antenna system 410 may not be present, and the signal output by the transponder 400 may be provided via direct connection to a DATA pad. In the main hereinafter, a transponder having a coil antenna, and used in the passive mode is described.

The transponder IC 402 includes interface circuitry 422 (compare 222) for processing an RF signal, such as an un-modulated carrier signal of frequency F_i (e.g., 125 kHz) received by the antenna 412, and for rectifying the received RF signal so that it can be used to power the transponder 400 operating in passive mode. The signal processing includes passing on a suitable form of the incoming signal to be used for generating timing/clock pulses for the transponder 400, and also includes applying modulation to the carrier signal for transmission by the antenna system 410.

The rectified carrier signal is clamped to a maximum of approximately 13.0 volts to prevent breakdown of the IC 402 substrate. The clamped, rectified signal has a voltage V_{pp} which can be read at a VPP pad, and ranges from 0 – 13 volts. The V_{pp} voltage is then shunt-regulated to a maximum of 6.5 volts, and designated as supply voltage (or "input voltage") V_{xx} which can be read at a VXX pad. The V_{xx} voltage level follows the V_{pp} voltage, and is about 6.2 volts for a typical received RF signal. Voltage V_{xx} is regulated to prevent voltages high enough to potentially damage CMOS circuitry in the IC 402.

The voltage V_{xx} is provided to a power-on reset (POR) circuit 482 (which is new to this model transponder), and also to a regulation and bandgap reference circuit 423 (compare 222) for providing various voltage supplies to the circuitry on the IC chip 402.

The power-on reset circuit 482 is provided to ensure that the transponder 400 will

not begin to record sensor readings or to transmit data until enough power is being supplied by the received carrier signal to allow proper functioning of the transponder 400. The POR circuit 482 evaluates the voltage V_{xx} level and outputs a reset signal which is not released until the V_{xx} voltage is deemed sufficient. If desired, such as for test purposes, the reset 5 signal can be imposed from outside the chip 402 through an RES connection pad.

In the passive mode, as long as the supply voltage V_{xx} is sufficient (at least 4 volts as determined by the POR circuit 482), the regulation and bandgap reference circuitry 423 will regulate voltage V_{xx} to provide a regulated analog supply voltage V_{cc} of approximately 3 volts, with an operating range of 2.8 V (minimum voltage for a stable oscillator 452) to 10 approximately 3.5 V. The digital supply voltage V_{dd} is regulated by a source follower connected to voltage V_{cc} and can supply current independently of voltage V_{cc} (compare with previous method as in Figure 3B, described hereinabove). Voltage V_{dd} is typically about one threshold below V_{cc} , or approximately 2.5 volts, ranging from 1.2 V (minimum voltage for stable logic and memory operation) to approximately 3.5 V, and supplies both 15 the digital logic and the EEPROM (memory) array 436 during reading. During transponder programming, voltages V_{cc} and V_{dd} are not affected by applying power to pad VPP. The voltages V_{cc} and V_{dd} can be read externally via their correspondingly-named connection pads (VCC and VDD). Also, in active (battery-powered) mode, the regulators can be overridden by applying external power to the VCC and VDD pads. Finally, for circuits 20 which need a stable reference voltage, the regulation and bandgap reference circuit 423 provides a temperature-independent bandgap voltage V_{bg} . The reference voltage V_{bg} is also independent of the chip supply voltage V_{xx} as long as the voltage V_{xx} is above a minimum operating level. The regulation and bandgap reference circuit 423 will output a substantially temperature-independent voltage V_{bg} of approximately 1.20 volts over a 25 transponder operating temperature range of, for example, -40 to 150 degrees C. The bandgap voltage V_{bg} is used as a reference voltage by the V_{xx} , V_{cc} and V_{dd} regulators 423 as well as the relaxation oscillator 452 and the power-on reset circuit 482.

The interface and rectification circuitry 422 also provides the received RF signal, 30 preferably at the input frequency (F_i) it is received, to a timing and clock generator circuit 424 (compare 224, 226) which generates clock signals in a known manner for controlling the timing of other circuits on the IC chip 402. The generated clock signal is a 50% duty cycle square wave, preferably at frequency F_i , and is independent of any modulation applied

to the antenna system 410 by the transponder 400 for the transponder's PSK transmission. The timing and clock generator circuit 424 also divides down the system clock to develop timing for addressing of the data in the addressable memory 438, and for the modulation. For example, the system clock frequency F_i is divided by two to determine the frequency of the PSK modulated return carrier signal. Other divisions of the frequency F_i are used for determining the baud rate for data transmission. In active or test modes of operation, the timing and clock generator circuitry can be bypassed or used as a buffer for direct input of the clock signal via a CLK pad or the VB antenna pad.

From the timing and clock generator 424 the various clock signals are passed to several control logic circuits: the column decoder 440 (compare 240), the column to data converter 441, and the row decoder & N_T , N_P control 442 (compare 242) which control access to data stored in the addressable memory 438. The clock signals are also used by the row decoder & N_T , N_P control 442 to control the timing of the relaxation oscillator 452 and the data capture circuitry 454, which generate and store the temperature N_T and pressure N_P readings (counts) in the temperature register 432 and pressure register 434. Thus the row decoder & N_T , N_P control 442 functions as a "timing generator" secondary to the timing and clock generator 424.

The addressable memory block 438 includes an EEPROM array 436 (compare 236) and several hardware registers 432, 434, and 435 (compare 232 and 234). The EEPROM 436 is programmed with a variety of stored information which will be described in detail hereinbelow.

The last two rows of the EEPROM (e.g., rows 14 and 15) constitute a trimming bits section 436b which is programmed to store trimming information. The trimming information: (a) controls the scaling of the current (in the base-emitter voltage to current converter 450) supplied to the relaxation oscillator 452 to optimize the pressure and temperature count resolution, (b) sets the modulation index in the modulation circuit 446 to optimize signal transmission for a given antenna system 410 and for a given transponder application, (c) sets the mode of operation (active or passive), and (d) optimizes the impedance of a clamp on the voltage V_{pp} across the rectification circuit 422. Utilizing the trimming lines 485, the trimming information stored in the trimming bits 436b can be directly read by the circuits it affects (e.g., 450, 446, 484, 422, 482) at any time during transponder operation (active or passive). Alternatively, as in certain test and programming

modes, the trimming bits 436b can be accessed for external reading and writing (programming) along with the rest of the EEPROM 436 memory via the DATA connection pad, as controlled by the test logic circuitry 484, and communicated by a transponder data line 444 through the column to data converter 441.

5 As described hereinabove with reference to the previous model transponder 200, the temperature and pressure registers (432 and 434 respectively) are each a hardware register holding the count (e.g., 12 bit) of a down-counter which is clocked by the sensor data signal of frequency F_{osc} coming from the sensor interface section 406.

10 The parity, MTMS 435 section of memory is also new to this model of transponder 400. It is implemented as a register in hardware with, for example, 12 bits of stored data. Five bits are permanently set (value = 1), then there is a bit which sets/clears according to the open/closed (1/0) status of the MTMS switch (closes if exposed to excessive 15 temperature), and finally six bits registering the parity of the pressure and temperature counts: three parity bits for the pressure register 434 count N_p , and then three parity bits for the temperature register 432 count N_t . The parity bits are continuously updated during sensor data capture, following the changing counts in the N_p and N_t down-counters (the pressure 434 and temperature 432 registers, respectively). Each parity bit represents the 20 parity of 4 sequential bits (a "nibble") in the corresponding pressure 434 or temperature 432 register; with the most significant parity bit representing the most significant nibble of the count, the middle parity bit for the middle nibble of the count, and the least significant parity bit for the least significant nibble of the count.

25 The sensor interface portion 406 (compare 206) of the transponder chip 402 consists of the base-emitter voltage to current converter 450 (compare 250) with connection pad "Rext"; the relaxation oscillator 452 (compare 252) with connection pad "Cp"; the data capture circuitry 454 (compare 254); and the "MTMS" connection pad and line 459 connecting it to the MTMS bit in the parity, MTMS register 435 (compare 236 for the previous location of the MTMS bit).

30 The base-emitter voltage to current converter 450 functions in a similar way to the converter 250 which is described in greater detail hereinabove with reference to sections 306 to 310 of Figure 3. For improved performance, the circuitry of sections 306, 308 and 310 in the new base-emitter voltage to current converter 450 utilizes cascodes instead of single stage current mirrors (e.g., for transistors P1, P2, P4, P6), and the external resistor Rext

416 may have a different preferred resistance value, such as 500 kilohms. Cascodes are
desirable because of their increased power supply rejection ration (PSRR). Also, in a
feature to be described more fully hereinbelow with reference to Figure 5, the final stage
510 (compare 310) of the base-emitter voltage to current converter 450 is connected in a
different way to section 308, and works in conjunction with programmed settings in the
trimming bits register 436b to provide a scaled proportional-to-temperature current $I(T)B$ on
the line 451, 511 (compare current $I(T)/N$ on line 251, 311) to the relaxation oscillator
circuitry 452 (compare 252). In contrast with the previous design, the current scaling circuit
510 (compare 310) can scale the current $I(T)$ by a variable scaling factor "B", as determined
10 by programmed settings in the trimming bits register 436b.

The relaxation oscillator 452, under the timing control of the row decoder & N_T, N_P
control circuit 442, works in conjunction with the external capacitive pressure sensor C_p
418 to generate a signal on line 453 (compare 253) with frequency $F_{osc'}$ which is indicative
of either the ambient temperature or the ambient pressure, depending on the timing window
15 determined by the row decoder & N_T, N_P control circuit 442. The data capture circuitry
454, under the timing control of the row decoder & N_T, N_P control circuit 442, directs the
 $F_{osc'}$ signal to the appropriate hardware register (depending on the timing window): to the
temperature register 432 via line 455, or to the pressure register 434 via line 457.

20 The current scaling circuit 510 (part of the base-emitter voltage to current converter
450) and the relaxation oscillator 452 have improvements compared to the relaxation
oscillator 252, and the MTMS 420 status is directed to a different memory location (register
435) than in the previous implementation (EEPROM 236). Otherwise, the sensor interface
section 406 functions essentially the same as the corresponding section 206 in the previous
model 3070C transponder 200.

25 As described hereinabove with reference to the previous model transponder 200, the
term "ambient" refers to the parameter being measured in the vicinity of the transponder
400, or more particularly in the vicinity of the respective sensors associated with the
transponder 400. Also, references made herein to "pressure readings", "pressure counts",
"pressure response", "pressure register" and the like generally refer to "pressure" as
30 measured by this transponder technique which actually produces a hybrid pressure-
temperature reading. When this hybrid reading has been processed to remove its
temperature component, the reading is referred to as a "pressure-only" reading.

In conjunction with the column decoder 440 and the row decoder 442, the column to data converter 441 controls the sequence in which signals (i.e., data) are output on a line 444 (compare 244) to a modulation circuit 446 (compare 246) which, via the interface and rectification circuitry 422 (compare 222), communicates selected measured tire operating 5 characteristics in a data stream via the antenna system 410 to an external reader/interrogator (e.g., 106). The line 444 also communicates the data stream to the test logic circuit 484 where it can be directly accessed via the DATA connection pad.

The modulation circuit 446 converts the data stream from line 444 to a representative sequence of impedance changes (modulations) which are applied to the antenna system 410 through the interface and rectification circuit 422. A new feature of the transponder 400 of 10 the present invention is the ability to modify the modulation index (magnitude of modulation) to suit operating power levels and to select (via the trimming bits 436b) a modulation index optimized for the individual transponder 400, antenna system 410, and reader/interrogator 106 in use.

15 In passive mode operation, an RF carrier signal from an external source (e.g., a reader/interrogator 106) is received by the antenna 412. This RF signal is rectified and used to power the RF transponder 400 as well as providing the timing/clock signals. Modulating information applied by the modulation circuit 446 is used to alter characteristics (e.g., impedance, resonant frequency, etc.) of the LC tank circuit of the antenna system 410. 20 These alterations are sensed as changes in load by the external reader/interrogator 106 and are decoded, providing communication of data back from the RF transponder 400 to the external reader/interrogator 106. Because the transponder 400 passive power is derived from the received RF signal, and because modulation of that signal drains off some of that power, the POR circuit 482 maintains a reset signal during passive power-up, and will not 25 clear the reset signal (thereby allowing modulation), until the transponder power levels are high enough to assure stable operation of the transponder 400 during modulation.

30 The test logic circuit 484 enables tests that can be performed at all phases of transponder production and use, including wafer sort, initial board assembly level programming, programming at the pre-calibration stage, calibration and trimming of the transponder, and post-calibration programming to adjust the trimming bits 436b for encapsulation-induced offset error.

More detailed explanations of significant portions of the RFIQ™ transponder 400 of

this invention are presented in the following sections.

MEMORY ASSIGNMENTS AND THE DATA STREAM

The addressable memory block 438 is organized in a way which provides a data stream that is improved over that of the previous model 3070C transponder 200. The 5 column decoder 440, the column to data converter 441, and the row decoder & N_T , N_P control circuit 442 work together to control the flow of data in and out of the addressable memory block 438. When operating in the active or passive modes (i.e., not in a test or programming mode), the circuits 440, 441 and 442 access the memory locations one at a time in sequence from the first address to the last (most significant bit to the least significant 10 bit in each data "word", with words sequenced from the lowest numbered word to the highest), thereby producing a serial string of data for transmission. It will be seen from the following description that the rows to be included in the data stream are selected according to the mode of operation (i.e., passive/active, or a variety of test and programming modes). An added function of the row decoder & N_T , N_P control circuit 442 is to control the sensor 15 interface circuitry 406 (via line 487) so that it is accumulating temperature-related counts in the temperature register 432 during one portion of the data transmission (e.g., while transmitting words/rows 2 through 6), and pressure-related counts in the pressure register 434 during another portion of the data transmission (e.g., while transmitting words/rows 9 through 13), both accumulations to be completed in time for the counts to be read back out 20 of the registers 432 and 434 when their part of the data stream is due (e.g., words 14 and 15).

Figure 4B (compare Figure 3C) is a "map" of the addressable memory block 438, showing its physical organization (by "rows") and also showing the organization of the active or passive mode data stream (by "words"). In the preferred embodiment of 25 transponder 400 described herein, each word or row is 12 bits (or columns) in length, and there are 16 words in the data stream, comprising a total of 192 bits (12 times 16). The drawing of the memory block 438 in Figure 4A is helpful in understanding the physical organization. It should be noted that the rows 1 to 13 of physical memory (EEPROM 436) correspond to the words 1 to 13 of the data stream, but the rows 14 and 15 of physical 30 memory (EEPROM 436) are not part of the data stream. Instead, the temperature register 432 is read out as word 14, and the pressure register 434 is read out as word 15 of the data stream. The final word of the data stream, word 16, is read out of a hardware register of

physical memory (the parity, MTMS register 435).

The EEPROM 436 portion of the exemplary addressable memory block 438 comprises 180 cells arranged in a 12 column by 15 row array. Each cell is made up of at least one n-channel select gate and one corresponding EEPROM transistor. The first 13 rows (sync, I.D., calibration, CRC 436a) are readable in the normal read modes whether the transponder 400 is programmed to be active or passive. The EEPROM memory locations in these first 13 rows are selected in the usual way, with one n-channel transistor row selection gate per EEPROM transistor. The EEPROM cells at rows 14 and 15 (trimming bits 436b) hold the data for 12 bits of trimming information, and are configured differently to facilitate their special role in the transponder. Each trimming bits 436b EEPROM cell has two gates instead of one, adding a special READ_TRIM selection gate in series with the row selection gate so that the trimming bits 436b cannot be added to the data stream unless the READ_TRIM selection gate has been enabled as in certain test modes of transponder operation. Another feature of the special trimming bits 436b register is that each trimming bits 436b cell also has an added sensing line to communicate the EEPROM bit setting (programmed trimming information) to appropriate sections of the transponder 400 circuitry as needed.

Thus the EEPROM 436 and associated logic are structured so that: The trimming bits 436b data can be read externally by a "READ_TRIM" test mode which reads out the bits sequentially as words 14 and 15 in the data stream in place of the temperature and pressure counts. In a "READ" test mode, as in normal operation, the trim bits are not seen in the data stream, but are still accessed by sense amplifiers to communicate programmed trim settings to appropriate sections of the transponder 400. In a "WRITE" test mode, all the EEPROM 436 cells (including the trim bits 436b) are addressed simultaneously and are written to. This in effect writes '1's to all the EEPROM cells, giving them high thresholds. In an "ERASE" test mode, individual cells can be erased (programmed to '0', given a low, negative, threshold): as the clock CLK signal indexes through the EEPROM cell array, a cell at the intersection of the column addressed and the row addressed is erased by raising the voltage on the VPP pad to the programming voltage and enabling the erasure by raising the DATA pad high.

Referring to figure 4B, the map illustrates an exemplary organization wherein the first twelve data locations (bits 000..011 in row 1) are reserved for synchronization ("sync")

data. The next forty-eight data locations (bits 012..059 in rows 2 through 5) are for general information identifying the individual transponder 400. As mentioned hereinabove, each transponder unit is suitably calibrated prior to its installation in a tire. The next twenty-four data locations (bits 060..083 in rows 6 through 7) hold temperature calibration data (e.g., a defining point and a slope). The next twenty-four data locations (bits 084..107 in rows 8 through 9) hold pressure calibration data (e.g., a defining point and a slope). The next thirty-six data locations (bits 108..143 in rows 10 through 12) hold additional identifying information concerning the IC chip 402. The next twelve data locations (in row 13) hold four bits of identifying information about the chip calibration (bits 144..147), and an eight bit value (bits 148..155) for a data validation algorithm such as CRC (Cyclic Redundancy Check). The next two words in the data stream (words 14..15, bits 156..179) are read from the temperature register 432 and the pressure register 434, respectively. The final word of the data stream (word 16, bits 180..191) is read from the parity, MTMS register 435, which contains five "open" bits (bits 180..184), then one bit (bit 185) containing the logic level (state) of the MTMS switch 420, and finally six bits (bits 186..191) containing 3 bits each for the parity of the pressure count followed by the parity of the temperature count. The five open bits are unused, and are fixed as logical "1" values.

20 The column decoder 440, column to data converter 441, and row decoder & N_T , N_p control 442 circuits coordinate addressing and access to the addressable memory block 438.

25 The column decoder 440 consists of a four-bit synchronous counter that addresses a 1-of-12 decoder. The outputs from the column decoder 440 address the 12 columns of the memory array during programming and reading. To address a column, the address n-channel device routes a low power current-source to charge the addressed column. If a bit is written to, the column will be pulled high, but if erased, the column will be pulled low. The output of the current-source is buffered and drives a transponder data line 444 that goes through the column to data converter 441 to the modulation 446 and test logic 484 circuits. The columns are sequentially addressed from column 1 to column 12 at the rate of a timing logic clock signal provided either by the timing and clock generator 424, or externally via the CLK pad. After addressing column 12, the column decoder 440 triggers the row decoder & N_T , N_p control 442 to clock it to the next row and also cycles itself back to column 1. Whenever a reset signal (turned on, then off) is received from the power-on reset circuit 482 (or via the RES pad), the column decoder 440 and the row decoder & N_T , N_p

control 442 will reset their addressing sequence to start at column 1 of row 1, i.e., the first bit or cell in the addressable memory block 438. The column decoder 440 serially addresses the EEPROM 436 array in any of the reading modes of operation or during erasing. In the WRITE test mode it has no effect, since the entire EEPROM memory is simultaneously addressed for the WRITE operation.

The row decoder & N_T , N_P control 442 is a 4-bit synchronous counter that addresses a 1-of-16 decoder. The decoder addresses 13 rows of EEPROM data memory 436a from rows 1 through 13. In the WRITE, ERASE, and READ_TRIM test modes, it also addresses rows 14 and 15 of the EEPROM memory 436b for the trimming bits. During normal reading (active or passive mode), the decoder addresses the temperature 432 and pressure 434 hardware registers at row addresses 14 and 15, respectively. Regardless of operating mode, the row-16 address is directed to a special data row: the parity, MTMS 435 hardware register. In the READ and ERASE test modes each row is addressed sequentially on the falling edge of the last bit of the column decoder 440. In the passive or active mode, a reset signal sets the row decoder & N_T , N_P control 442 to row 1, which is the sync word. In the WRITE mode, all the rows are simultaneously addressed, which pulls all select lines and control gates to voltage V_{pp} . As mentioned hereinabove, an added function of the row decoder & N_T , N_P control circuit 442 is to control the sensor interface circuitry 406 so that it is accumulating temperature-related counts in the temperature register 432 and pressure-related counts in the pressure register 434 during their designated time periods (data collection windows).

POWER-ON RESET

When operating in the passive mode, power levels in the transponder are susceptible to variations resulting from varying levels of coupling between the transponder antenna 210, 410 and a reader/ interrogator antenna (e.g., 110). For example, power to the transponder will vary with the distance between a transponder 102, 200, 400 in a tire 104 and a handheld reader/interrogator 106 as it is brought near the tire 104 from a "far-field" distance. When operating in a battery-powered (active) mode, similar low power problems will occur when the battery voltage drops off near end of life. At low power levels, the relaxation oscillator 252, 452 output F_{osc} can yield lower frequencies (see Figure 3D) in a way unrelated to the temperature and pressure being measured, thereby causing erroneous temperature and pressure counts N_T and N_P . As described hereinabove, this problem can be partially

compensated for by using a ratio of counts N_T / N_P to indicate the pressure measurement. At very low power levels, the voltage regulation circuitry 222, 423 cannot provide voltage levels sufficient to assure stable functioning of the analog and digital components of the transponder 200, 400, making the output of the transponder 200, 400 erratic and unpredictable.

5 According to the invention, these problems are addressed with the provision of a Power-On Reset Circuit 482 (POR) in the new RFIQ™ transponder 400 design. The POR 482 circuitry is schematically illustrated as the POR circuit 600 in Figure 5. The POR 482 ensures that:

- 10 1. The bandgap voltage V_{bg} is stable;
2. Analog and digital supply voltages V_{cc} and V_{dd} are regulated and will be stable;
3. All chip digital functions and addressing will be stable;
4. The relaxation oscillator 452 will be stable, and will start operating in a known state;
- 15 5. The output data stream will begin at bit 1, and will include complete, valid measurement counts N_T and N_P , thereby allowing a complete data reading in a single pass immediately after start of transmission;
6. The transponder 400 has sufficient power (as indicated by the voltage level V_{xx} of the input power) to modulate the antenna 410, without drawing down the regulated voltages below their stable operating limits.

20 The POR 482 will generate a reset signal RESET for the transponder circuitry 400 in any operating mode: testing, passive and active. An external connection pad, labeled "RES", is available to optionally input an external reset EXT_RES for testing and in the active modes. The externally-supplied reset EXT_RES is "OR-ed" with the internally-generated reset INT_RES, to produce the circuit-wide reset signal RESET. The external reset EXT_RES is also pulled back to ground if the voltage V_{dd} is at a sufficient level to operate CMOS logic.

25 The reset signal RESET is generated by the POR 482 under both power-up and power-down conditions, and behaves differently depending on the rate of power change, and also on the mode of operation. In active (battery-powered) mode, the reset signal will be high for a very short time (e.g., 10 - 20 μ sec) when a battery is connected to the transponder 400 (assuming the battery outputs more than a low-battery voltage limit $V_{sustain(active)}$ -

e.g., 2.75 V) . As the battery voltage drops over life, the reset signal is again set high when the battery voltage drops below the low-battery voltage limit Vsustain(active), and the reset signal will remain high (holding the transponder 400 in an inoperative reset mode) until the voltage drops too low to allow any effective transponder 400 functioning.

5 In passive mode, where power is derived from the RF carrier signal input to the transponder antenna 410, there are three scenarios for power-up and power-down: (a) The RF power changes abruptly, as when a reader/interrogator 106 is close to the transponder 400 when it begins or abruptly stops transmitting its RF interrogation signal; (b) The RF power changes somewhat slowly, as when a transponder 400 in a tire 104 moves quickly 10 past a fixed reader/interrogator 106 which is transmitting continuously; (c) The RF power changes gradually, as when a transmitting handheld reader/interrogator 106 is slowly walked past a transponder 400. These scenarios can be combined to achieve, for example, fast power-up plus slow power-down.

15 For the passive mode of operation, the POR 482 uses two different minimums for the voltage Vxx (derived from the RF carrier signal input power). The lower-valued minimum, Vsustain(passive), is a minimum Vxx voltage level (e.g., 4.0 V) which is sufficient to assure that all power supply voltages are adequate to sustain stable transponder 400 operation. Since modulation of the antenna 410 for transmission represents a significant drain on the power available to the transponder 400, there must be a higher-valued minimum 20 Vstart (e.g., 4.5 V) used when powering up, in order to assure that there is sufficient reserve power to modulate the antenna 410 without dragging the power supply voltages below a level adequate to sustain stable transponder 400 operation.

25 For abrupt power-up in passive mode (which is the same as attaching a sufficiently-charged battery in active mode), the POR 482 will turn on the RESET signal immediately (upon detection of the voltage Vxx above the minimum Vstart) and will turn it back off (release the RESET signal) after a delay time Ramp_Delay (e.g., approximately 10 - 20 μ sec), thereby allowing time for transponder 400 operational stability before starting data stream transmission at bit 1.

30 Although due to different circuit logic, the results of either somewhat slow or gradual power-up are the same: the POR 482 will turn on the RESET signal as soon as the voltage Vxx has developed to a level sufficient to generate the bandgap voltage Vbg which is needed to stably power the circuitry in the POR 482, and will turn it back off (release the

RESET signal) after the voltage V_{xx} has exceeded the minimum V_{start} in passive mode or the minimum $V_{sustain(active)}$ in active mode. The distinction between "somewhat slow" and "gradual" depends on the time period for the voltage V_{xx} to increase from zero to V_{bg} volts, with a gradual rate taking significantly more time than the Ramp_Delay time (e.g., 10 times as much).

In passive mode power-down situations, regardless of the rate of voltage drop, the POR 482 will again turn on the RESET signal immediately upon detection of the voltage V_{xx} below the minimum $V_{sustain(passive)}$, and will not release it until the transponder 400 has ceased to function altogether due to lack of power. This halts modulation, and therefore 10 halts transmission of potentially erroneous data while the transponder is unstable due to excessively low power supply voltages. If the RF power is wavering in a way which brings the voltage V_{xx} back up after momentarily dropping below the minimum $V_{sustain(passive)}$, the POR 482 will not release the RESET signal until the voltage V_{xx} rises above the higher startup minimum level of V_{start} . This hysteresis effect prevents an erroneous data stream 15 due to unstable on-off oscillation, or "hiccup" in the transponder 400 transmission when operating in marginal RF signal reception conditions.

The POR 482 circuit will now be described with reference to Figure 5 which is a schematic block diagram of the POR 482 circuitry 600.

Inputs to the POR circuit 600 are shown on the left, including the external reset 20 signal EXT_RES input via connection pad RES; the rectified and limited input voltage V_{xx} extracted from an RF carrier signal received by antenna 410 via the interface & rectification circuit 422; the digital voltage supply V_{dd} and the bandgap voltage V_{bg} which are derived from the input voltage V_{xx} by the regulation and bandgap reference circuit 423; a bias voltage P_{bias1} generated by a V_T -referenced current mirror arrangement in the regulation 25 and bandgap reference circuit 423; and the stored setting of trim bit 4 in the EEPROM trimming bits register 436b, communicated via lines 485. The value of the trim bit 4 setting, designated "TRIMBIT_4," is "set" or logical "1" if the transponder 400 has been programmed to be in the active mode, and "cleared" or logical "0" if the transponder 400 has been programmed to be in the passive mode. The logic signals in the schematic 600 are 30 labeled with names suggestive of their "true" or set state. For example, the TRIMBIT_4 signal is also called the "ACTIVE" signal, but when passed through an inverter, the inverted TRIMBIT_4 signal becomes the "PASSIVE" signal. The inverted ACTIVE signal could

also be designated the "ACTIVE" signal, using the common notation of a line over the logic signal name for inverted, or "NOT" logic signals. In the cases of the signals V_START and V_SUSTAIN, the signal names indicate that the voltage Vxx has exceeded the corresponding minimum voltage level, Vstart or Vsustain, respectively.

5 The main output of the POR circuit 600 is the RESET signal shown on the right with a truncated line which leads to other sections of the transponder circuit 400 as needed. It can be seen that the NOR gate 658 combined with the following inverter 633c form an OR gate which effectively outputs a high RESET signal whenever either the externally-set EXT_RES or internally (POR)-determined INT_RES reset signal is high. Thus either the 10 INT_RES or the EXT_RES reset signal can turn on the RESET signal, but both must agree to turn off the RESET signal. It can be seen that a transistor such as the illustrated N-channel transistor N30 can be used to pull down (turn off) the EXT_RES signal as soon as the voltage Vdd has developed to a high enough level to operate the transistor N30.

15 Mostly standard symbols are used for the logical elements of the schematic 600, but it must be noted that in addition to the normal type of inverter 633a..633f (633), there are several Schmitt trigger inverters 631a..631d (631), indicated by a hysteresis curve inside the triangle of a standard inverter symbol. The Schmitt trigger inverters 631 are used to "square up" the transitions between logic levels and prevent any "crowbar" effects since these transitions are dependent on analog inputs which may be varying at slow rates.

20 The element 632 is illustrated in a simplified way as a double-throw switch. The switch 632 is representative of a set of semiconductor elements, such as P-channel and N-channel transistors combined in a manner known to those of ordinary skill in the arts which pertain. The semiconductor switch 632 uses indirect means to switch one of the analog voltages Vxx/A or Vxx/B to the positive (+) input of the comparator 638, depending on the 25 logical setting of the trim bit 4.

25 The circuit portion labeled "620" is an init delay circuit; the portion labeled "640" is a voltage limit circuit; and the portion labeled "650" is a flip-flop circuit. Various voltages are handled in the mainly analog circuitry of circuits 610, 620, and 632 and then the voltages are used by the comparators 634, 636, and 638 to determine logic signals V_INIT, 30 V_START, and V_SUSTAIN, respectively, which are used by the logic circuits 640 and 650 to determine an internal reset signal INT_RES.

Because the POR circuit 600 must function as soon as possible while the power input

to the transponder 400 is still building up from very low levels, many measures have been employed to enable functioning at unusually low power supply levels. For example, the comparators 634, 636, and 638 are three-stage, low current (e.g., 300 nano-amp) comparators which have a good power supply rejection factor. Also, as in other circuitry 5 described hereinabove, the comparators 634, 636, and 638 utilize current mirrors and may also employ cascode configurations. The current mirrors are controlled by Pbias1 inputs (which could be Pbias1' and Pbias1'' in the case of cascode usage). The Pbias1 input is developed in the regulation and bandgap reference circuit 423 utilizing a V_T -referenced current mirror. The V_T -referenced current mirror is a known device which operates stably 10 at the low voltage of 1.2 V and will generate a bias voltage Pbias1 which is one threshold drop below the input voltage Vxx. If the V_T -referenced current mirror is implemented in a cascode form, it can generate two bias voltages Pbias1' and Pbias1'' which have voltage levels of one and two threshold drops, respectively, below the input voltage Vxx. In 15 addition to supplying the comparators 634, 636, and 638, the bias voltage Pbias1 (or Pbias1' and Pbias1'') is(are) used to control the gate(s) of the current mirror transistor(s) P30 in an init delay circuit 620 (which can also be implemented as a cascode of, for example, two transistors P30' and P30'' controlled by bias voltages Pbias1' and Pbias1''). Since Vxx is 20 the highest available rectified and regulated voltage supply (with voltage level "Vxx") in the transponder 400 circuitry during power-up, it is supplied to power the comparators 634, 636, and 638 so they can function as early as possible during power-up. The bandgap voltage Vbg is the lowest (and therefore earliest to be developed during power-up) stable voltage suitable for use as a reference voltage and is supplied for that purpose to the negative (-) inputs of the comparators 634, 636, and 638.

A voltage divider circuit 610 comprises a multi-element voltage divider which 25 utilizes on-chip high value poly resistances to divide-down the input voltage Vxx to create relative voltages for use in the comparators 636 and 638. By known, low-current techniques, the voltage Vxx is divided by a small factor A to create voltage V_{xx}/A , by a larger factor B to create voltage V_{xx}/B , and by an even larger factor C to create voltage V_{xx}/C . It can be seen that when comparator 636 compares voltage V_{xx}/C to voltage Vbg, 30 the comparator 636 output will go high when $V_{xx}/C > V_{bg}$. This is mathematically equivalent to having voltage Vxx greater than voltage Vbg times the factor C. Since the comparator 636 is intended to determine when the voltage Vxx exceeds the minimum

passive starting voltage V_{start} , the resistances in the voltage divider are adjusted to divide down V_{xx} by a suitable factor C which will make C times V_{bg} equal to voltage V_{start} . For example, if voltage V_{bg} equals 1.2 V, and if voltage V_{start} equals 4.5 V, then factor C equals 3.75, and the voltage divider 610 will divide the incoming voltage V_{xx} by 3.75 to 5 create the voltage V_{xx}/C mathematically equal to $V_{xx}/3.75$.

The comparator 638 determines when the voltage V_{xx} exceeds the minimum sustaining voltage level $V_{sustain(active)}$ or $V_{sustain(passive)}$, whichever is appropriate for the operating mode. The factors A (for active mode sustaining voltage) and B (for passive mode sustaining voltage) are determined as described above. For example, if voltage V_{bg} 10 equals 1.2 V, and if voltage $V_{sustain(active)}$ equals 2.75 V (the low-battery voltage limit), then factor A equals approximately 2.29, and the voltage divider 610 will divide the incoming voltage V_{xx} by approximately 2.29 to create the voltage V_{xx}/A which is mathematically approximately equal to $V_{xx}/3.75$. Finally, for example, if voltage V_{bg} 15 equals 1.2 V, and if voltage $V_{sustain(passive)}$ equals 4.0 V, then factor B equals approximately 3.33, and the voltage divider 610 will divide the incoming voltage V_{xx} by approximately 3.33 to create the voltage V_{xx}/B which is mathematically approximately equal to $V_{xx}/3.33$.

The switch 632 will connect the voltage V_{xx}/A to the comparator 638 if the transponder is in active mode, as determined by a TRIMBIT_4 value of logical 1 (ACTIVE = TRUE). If the transponder is in passive mode, as determined by a TRIMBIT_4 value of 20 logical 0, then the inverter 633d will invert the logic to become PASSIVE = TRUE which causes the switch 632 to connect the voltage V_{xx}/B to the comparator 638.

The flip-flop circuit 650 is comprised of a well-known set-reset latch 656 (the interconnected NOR gates 656a and 656b) combined with a front end NOR gate 652 and 25 NAND gate 654 which determine the switching logic. The set-reset latch 656 holds the state of the internal reset signal INT_RES until it is caused to change state by the logic in the rest of the POR circuit 600.

The voltage limit circuit 640 contains the logic to evaluate the signals INT_RES, 30 PASSIVE, V_SUSTAIN, and V_START, and determine when to trigger a change of state in the flip-flop circuit 650. The V_INIT signal is output by the comparator 634 to trigger changes in the flip-flop circuit 650 either upon initial power-up or after a delay during certain power-up scenarios as detailed hereinabove.

The init delay circuit 620 uses the current mirror transistor P30 to control the charging of the capacitor C3 by the input voltage Vxx. The voltage level of the charging capacitor C3 is Vxx' and this voltage is directed to the positive input of the V_INIT comparator 634. The capacitor C3 is sized (e.g., 5 – 10 pf) to produce a suitable
5 Ramp_Delay time as explained hereinabove.

To illustrate the operation of the POR 600 circuitry, consider the scenario of somewhat slow power-up. As voltage Vxx slowly increases from 0 volts, the Pbias1 voltage will follow, and will reference a small current through transistor P30 to slowly charge capacitor C3. Until voltage Vxx is sufficient to fully generate the bandgap voltage Vbg, the
10 bandgap voltage level will be low and unstable, as will the operation of the comparators 634, 636, and 638 and the logic elements. The capacitor C3 will cause the voltage Vxx' at the positive (+) input of the comparator 634 to lag behind the building bandgap voltage Vbg on the negative (-) input of the comparator 634, thereby preventing any action by the POR
15 circuitry 600 while it is in an unstable condition. Since the voltages in the rest of the transponder 400 circuitry are too low to enable any significant functioning, the absence of a
RESET signal at this point is irrelevant.

Once the voltage Vxx has increased enough to allow the development of a stable bandgap voltage Vbg, the POR circuitry 600 will be functional, but the capacitor C3 has been causing the voltage Vxx' at the comparator 634 positive input to lag behind the voltage
20 Vbg at the negative input, so the first stable output of the comparator 634 will be V_INIT low (logical 0). After double inversion by the Schmitt trigger inverter 631b plus the inverter 633b, this causes a 0 input to the NAND gate 652 which yields a 1 output to the NOR gate 656a regardless of the other input to gate 652. Likewise, the 1 input to the NOR gate 656a yields a 0 output to NOR gate 656b, regardless of the other input to gate 656a.
25 Simultaneously, the V_INIT signal is inverted by the Schmitt trigger inverter 631b and presented as a high (logical 1) input to NOR gate 654, which yields a 0 output to the NOR gate 656b regardless of the other input to gate 654. Thus the NOR gate 656b has logical zeros presented to both of its inputs which causes it to output a logical 1 or high value for
30 the flip-flop circuit 650 output signal INT_RES. This causes a high RESET signal to be output from the POR circuit 600 as soon as it is functional.

The high-valued INT_RES signal is also fed back to the voltage limit circuit 640 as an input to NAND gate 644. At this point in time, the voltage Vxx is much lower than

either the starting voltage or the sustaining voltage, so the comparators 636 and 638 will have low (logical 0) outputs for both the V_START and the V_SUSTAIN signals. These signals are inverted by the Schmitt trigger inverters 631c and 631d, producing logical 1 inputs to the voltage limit circuit 640. Thus the NAND gate 642 will have both inputs high, 5 yielding a 0 output to the NAND gate 646, which will cause the NAND gate 646 to yield a 1 output regardless of its other inputs. The logical 1 is directed to the other input of the NOR gate 654 in the flip-flop circuit 650, and is also inverted by inverter 633e and directed as a logical 0 to the other input of the NAND gate 652 in the flip-flop circuit 650.

The NAND gate 648 in the voltage limit circuit 640 plays a fail-safe role for the 10 POR circuit 600. It can be seen that with its inputs of ACTIVE, $\overline{V_SUSTAIN}$, and V_START, the NAND gate 648 will always output a logical 1 under normal operating conditions. The input voltage Vxx cannot be lower than the minimum voltage level Vsustain ($\overline{V_SUSTAIN} = 1$) and simultaneously higher than the minimum voltage level Vstart ($V_START = 1$), especially in active (battery-powered) mode (ACTIVE = 1). 15 Therefore, in order to obtain all-true inputs to gate 648, the voltage divider circuit 610 and/or at least one of the comparators 636 and 638 would have to be mal-functioning. The logical 0 output from NAND gate 648 which would result from such a malfunction would be directed to an input of NAND gate 646, holding gate 646 to a logical 1 output which would in turn hold the flip-flop circuit 650 in a state which keeps the INT_RES signal on 20 (and thus the RESET signal as well). In normal operation (and also in passive mode) the NAND gate 648 will always output a logical 1 to the NAND gate 646, and thus has no control over the functioning of gate 646. The function of the NAND gate 648 is the same in all power change scenarios, and should be understood as included in the descriptions herein, even if not repeated in the descriptions to follow hereinbelow.

25 The initial logic state settings for the POR circuit 600 are completed as the 1-valued inverted V_START signal ($\overline{V_START}$) is also directed to the NAND gate 644. Since the NAND gate 644 has two of its three inputs set to 1 (INT_RES and $\overline{V_START}$), its output will be controlled by the third input, the PASSIVE signal (the trim bit 4 setting inverted by the inverter 633d). If the transponder is in the passive mode, making the PASSIVE signal 30 true (logical 1), the NAND gate 644 will output a 0 to the NAND gate 646. If the transponder is in the active mode, making the PASSIVE signal false (logical 0), the NAND

gate 644 will output a 1 to the NAND gate 646.

It can be seen that since the NAND gate 652 at the front end of the flip-flop circuit 650 has zeros at both of its inputs, and since the NOR gate 654 at the front end of the flip-flop circuit 650 has ones at both of its inputs, the flip-flop circuit 650 will not change state 5 until both the V_INIT comparator 634 and the voltage limit circuit 640 changes state. It should also be noted that the RESET signal could have been turned on due to the inputs from the voltage limit circuit 640 (caused by the low outputs from the V_START and $V_SUSTAIN$ comparators 636 and 638, respectively) regardless of the state of the V_INIT comparator 634.

10 In the scenario being considered (somewhat slow power-up), the RESET signal will be turned off when the flip-flop circuit 650 changes state. The V_INIT comparator 636 will change state (to $V_INIT = 1$) when the input voltage V_{xx} has charged the capacitor C_3 (delayed by the charging time, $Ramp_Delay$) enough for the voltage V_{xx}' at the positive input of comparator 634 to exceed the now-stable reference voltage V_{bg} at the negative input of comparator 634. The outputs of the voltage limit circuit 640 must also change, and this cannot happen unless the inputs to the NAND gate 646 are all 1. The gate 646 input from the NAND gate 642 will change to 1 as soon as either of the comparators 636 and 638 go to a high output (i.e., the voltage V_{xx} has exceeded either of the voltages $V_{sustain}$ or V_{start}). The gate 646 input from the NAND gate 644 will change to 1 if any of three 15 conditions are at logical 0: the INT_RES signal, the $PASSIVE$ mode signal, and the V_START signal. At this point in the scenario, the INT_RES signal is still 1, so if the transponder 400 is in passive mode ($PASSIVE = 1$) then the voltage V_{xx} must exceed the voltage V_{start} causing the comparator 636 to output a high value for V_START , making the inverted signal low ($V_START = 0$). If the transponder 400 is in the active mode 20 ($PASSIVE = 0$), then the V_START signal is irrelevant (but the voltage V_{xx} must still exceed at least the voltage $V_{sustain}$ (active) to maintain the state of the NAND gate 642).

25 Thus the RESET signal is turned off (low) when the voltage V_{xx} has increased to a level above the minimum required for the operating mode of the transponder 400: V_{start} for passive mode, and $V_{sustain}$ (active) for active mode. It can be seen that since the NAND gate 652 at the front end of the flip-flop circuit 650 has ones at both of its inputs, and since the NOR gate 654 at the front end of the flip-flop circuit 650 has zeros at both of its inputs, 30

the flip-flop circuit 650 is primed to change state (turning the RESET signal back on) if either the V_INIT comparator 634 or the voltage limit circuit 640 changes state. With the RESET signal off, the transponder 400 can operate normally, as described hereinabove.

During normal transponder operation, the input voltage Vxx can rise in level without affecting any of the logic states in the POR circuit 600. If the input voltage Vxx level drops, the voltage limit circuit 640 will change its output state, and therefore the state of the flip-flop circuit 650 (re-activating the RESET signal) as soon as the input voltage Vxx drops below the minimum sustaining voltage level Vsustain(active) or Vsustain(passive) according to the transponder 400 operating mode, regardless of the rate of voltage drop. Since the 5 INT_RES signal changed to 0 when the RESET signal was turned off, the NAND gate 644 at the front end of the voltage limit circuit 640 has been forced to a logical 1 output to the second input of the NAND gate 646, regardless of transponder operating mode, thereby priming the NAND gate 646 to change its output (and the state of the voltage limit circuit 640) if its first input changes from logical 1 to 0. The first input to the NAND gate 646 is 10 controlled by the NAND gate 642 which will change its output to 0 only when both its inputs change to 0, i.e., when the voltage Vxx drops below both of the minimum voltage levels: the minimum starting voltage level Vstart, and the minimum sustaining voltage level Vsustain(active) or Vsustain(passive) according to the transponder 400 operating mode. The third input to the NAND gate 646, coming from the NAND gate 648 is the fail-safe signal 15 which is normally constant at 1, having no controlling effect.

20

For the scenario of gradual voltage increase, the only change to the scenario described hereinabove (for somewhat slow voltage increase) is in the effect of the init delay circuit 620. If the input voltage Vxx is increasing at a slow enough rate, the capacitor C3 will charge fast enough to maintain the voltage Vxx' at approximately the same level as the voltage Vxx, thereby making the positive input to the comparator 634 always higher than its negative input, so that the V_INIT signal output from the comparator 634 will be high as 25 soon as the comparator 634 is functional. This means that the output state of the gates 652 and 654 at the front end of the flip-flop circuit 650 will depend on the output states of the voltage limit circuit 640. As soon as the logic elements in the POR 600 circuitry become 30 functional, the NAND gate 642 will be driven to a zero output since its $\overline{V_START}$ and $\overline{V_SUSTAIN}$ inputs will both be logical ones. The logical 0 which this presents to the first

input of the NAND gate 646 will force the gate 646 output to 1 regardless of its second input, and therefore independent of the transponder 400 operating mode or RESET state. The logical 1 output from the NAND gate 646, and the logical 0 resulting from its inversion by the inverter 633e form the outputs of the voltage limit circuit 640 which are directed to the front end gates 654 and 652, respectively, of the flip-flop circuit 650. These inputs to the flip-flop circuit 650 are sufficient to force the flip-flop circuit 650 to output a high INT_RES signal, and therefore to turn on the RESET signal as soon as the input voltage Vxx became high enough to make the POR circuit 600 functional.

Finally, for the scenario of abrupt power-up (to a Vxx voltage level above voltage Vstart level for passive mode, or above the Vsustain(active) level for active mode), the init delay circuit 620 plays a different role, determining both the setting and the clearing of the INT_RES and thus the RESET signals. In this scenario, the voltage limit circuit 640 is immediately "cleared" to output a logical 0 to the NOR gate 654 and the inverse (a logical 1) to the NAND gate 652, because of the logical 0 provided by the $\overline{V_SUSTAIN}$ signal to an input of the NAND gate 642, and the logical 0 provided to an input of the NAND gate 644 by either the $\overline{V_START}$ signal in passive mode, or by the PASSIVE signal (being false) in active mode. These voltage limit circuit 640 outputs, which are input to the front end of the flip-flop circuit 650, enable the front end gates 652 and 654 to be controlled by their inputs from the V_INIT comparator 634. Upon abrupt power-up, the V_INIT comparator 634 will have a low output as soon as it begins to function, because its negative input voltage (Vbg) will be higher than its positive input voltage Vxx' which is lagging behind while the capacitor C3 is charged. A low V_INIT signal provides a logical 0 to the NAND gate 652, and a logical 1 to the NOR gate 654. As detailed above, these inputs are sufficient to force the output of the flip-flop circuit 650 to be set, thus turning on the INT_RES and the RESET signal immediately after the POR circuit 600 begins to function. Although the INT_RESET signal is fed back to the voltage limit circuit 640, it has no effect on the output of the voltage limit circuit 640 as long as the input voltage Vxx is above the appropriate minimum voltage level Vsustain. After the amount of time (Ramp_Delay) it takes to charge the capacitor C3 enough to make the voltage Vxx' greater than Vbg, the V_INIT comparator 634 will change state to a high output signal V_INIT. Since this signal is still controlling the front end of the flip-flop circuit 650, the V_INIT high signal will cause the flip-flop circuit 650 to change

state again, now clearing its output and thus turning off the INT_RES and therefore the RESET signals. As explained hereinabove, the present state of the logic gates will remain until the input voltage level Vxx drops down below the appropriate minimum sustaining voltage level: Vsustain(active) or Vsustain(passive), depending on the mode of transponder 5 400 operation. When the input voltage level Vxx drops this low, regardless of rate, the voltage limit circuit 640 will change state, forcing the flip-flop circuit 650 to change state, thereby turning on the INT_RES and the RESET signals until either the transponder 400 stops functioning entirely (as power drops further), or else the power comes back up enough to raise the input voltage level Vxx high enough to meet the startup conditions outlined 10 hereinabove.

15 Although the invention has been illustrated and described in detail in the drawings and foregoing description, the same is to be considered as illustrative and not restrictive in character, it being understood that only preferred embodiments have been shown and described, and that all changes and modifications that come within the spirit of the invention are desired to be protected. Undoubtedly, many other "variations" on the "themes" set forth hereinabove will occur to one having ordinary skill in the art to which the present invention most nearly pertains, and such variations are intended to be within the scope of the invention, as disclosed herein.

CLAIMS:

1. An RF transponder (102, 200, 400) comprising a plurality of circuits (200, 400), and a power supply (222, 422, 423) for providing power (V_{xx}, V_{cc}, V_{dd}), including an input voltage (V_{xx}), to the plurality of circuits, the RF transponder characterized in that:

5 a one of the plurality of circuits comprises a Power-On Reset (POR) circuit (482, 600) for generating a reset signal (INT_RES, RESET) for maintaining other ones of the plurality of circuits in an inoperative reset mode unless the power supply has sufficient power (V_{start}, V_{sustain}) to ensure proper operation of the other ones of the circuits; and

10 at least one of the other ones of the plurality of circuits comprises control logic (440, 442) which, upon release of the reset signal, starts transmission of a data stream at a first bit of the data stream, in order to ensure a first-pass transmission of a complete data stream.

2. An RF transponder, according to claim 1, characterized by:

15 a flip-flop circuit (650) for setting and clearing a state of the reset signal; and an init delay circuit (620), connected to an input of a comparator (634), for controlling the flip-flop circuit so that the flip-flop circuit holds the reset signal in an ON-state for a delay time (Ramp_Delay) after abrupt power-up of the transponder.

3. An RF transponder, according to claim 1, characterized by:

20 a flip-flop circuit (650) for setting and clearing a state of the reset signal; and a voltage divider (610) connected to a first comparator (638), for providing an input signal (V_SUSTAIN) to a voltage limit circuit (640); wherein the voltage limit circuit controls the flip-flop circuit so that the flip-flop circuit sets the reset signal in response to the input voltage being less than or equal to a minimum sustaining voltage (V_{sustain}), and clears the reset signal in response to the input voltage being greater than the minimum sustaining voltage.

25 4. An RF transponder, according to claim 3, characterized in that:

the minimum sustaining voltage has different values (V_{sustain}(active), V_{sustain}(passive), V_{start}) in different transponder operating modes (active, passive).

5. An RF transponder, according to claim 4, characterized in that:

30 in an active transponder operating mode, the power supply derives power for the plurality of circuits from a battery; and

in a passive transponder operating mode, the power supply derives power for

the plurality of circuits from an RF signal received by an antenna system (210, 410).

6. An RF transponder, according to claim 3, characterized by:

5 a second comparator (636) connected to the voltage divider and providing an input signal (V_START) to the voltage limit circuit; wherein the voltage limit circuit controls the flip-flop circuit so that the flip-flop circuit sets the reset signal while the input voltage is increasing from less than or equal to a minimum sustaining voltage (Vsustain) to a minimum starting voltage (Vstart), and clears the reset signal when the input voltage increases above the minimum starting voltage.

7. An RF transponder, according to claim 6, characterized by:

10 logic (633f, 642, 644, 646, 648, 633e) in the voltage limit circuit for combining the input signal from the first comparator and the input signal from the second comparator so that, after the input voltage has increased above the minimum starting voltage, the flip-flop circuit maintains a cleared reset signal state as long as the input voltage remains above the minimum sustaining voltage, and so that after the input voltage has 15 increased above the minimum starting voltage, the flip-flop circuit sets the reset signal when the input voltage decreases to less than or equal to the minimum sustaining voltage.

8. An RF transponder, according to claim 3, characterized by:

20 an init delay circuit (620) connected to an input of a second comparator (634) which shares control of the flip-flop circuit with the voltage limit circuit, so that the flip-flop circuit holds the reset signal in an ON-state after the beginning of power-up for a longer one of a first period of time which is a delay time (Ramp_Delay) and a second period of time which is a time expended while the input voltage increases to greater than a minimum voltage (Vsustain, Vstart).

9. An RF transponder, according to claim 1, characterized by:

25 an input (RES) for an external reset signal (EXT_RES); and at least one logic element (658, 633c), for combining the external reset signal with the POR-generated reset signal (INT_RES) and forming a combined reset signal (RESET), wherein the combined reset signal is set in response to either the external reset signal or the POR-generated reset signal being set, and the combined reset signal is cleared 30 when the external reset signal and the POR-generated reset signal are both clear.

10. An RF transponder, according to claim 9, characterized by:

a gate (N30) connected between ground and the input for the external reset

signal, wherein the gate is controlled by a one (Vdd) of the power supply voltages so that the external reset signal is cleared when the power supply voltage is at a level suitable for logic control.

11. An RF transponder, according to claim 1, characterized in that:

5 the power for the POR circuitry is the highest available regulated voltage (Vxx); and

components of the Power-On Reset circuit are selected for minimal power use and for operation at the lowest possible voltages, so that the Power-On Reset circuit is functional before the other ones of the plurality of circuits.

10 12. An RF transponder, according to claim 11, characterized in that the Power-On Reset circuit comprises:

low current, three-stage comparators (634, 636, 638);

Schmitt trigger inverters (631b, 631c, 631d); and

a low current voltage divider (610), utilizing on-chip, high value poly

15 resistances.

13. Method of controlling operation of an RF transponder (102, 200, 400) during power-up and power-down, wherein the RF transponder comprises a plurality of circuits (200, 400) and a power supply (222, 422, 423) for providing power (Vxx, Vcc, Vdd), including an input voltage (Vxx), to the plurality of circuits, the method characterized by:

20 generating a reset signal (INT_RES, RESET) for maintaining selected ones of the plurality of circuits in an inoperative reset mode unless the power supply has sufficient power (Vstart, Vsustain) to ensure proper operation of the plurality of circuits; and

25 upon release of the reset signal, starting data transmission with a first bit of a data stream to be transmitted, in order to ensure a first-pass transmission of a complete data stream.

14. Method, according to claim 13, characterized by:

holding the reset signal on for a delay time (Ramp_Delay) after abrupt power-up of the transponder.

30 15. Method, according to claim 13, characterized by:

setting the reset signal in response to the input voltage being less than or equal to a minimum sustaining voltage (Vsustain), and

clearing the reset signal in response to the input voltage being greater than the minimum sustaining voltage.

16. Method, according to claim 15, characterized by:

5 selecting a value for the minimum sustaining voltage to different values (Vsustain(active), Vsustain(passive), Vstart) for transponder operation based on different operating modes (active, passive) for the RF transponder.

17. Method, according to claim 16, characterized in that:

in an active transponder operating mode, the power supply derives power for the plurality of circuits from a battery; and

10 in a passive transponder operating mode, the power supply derives power for the plurality of circuits from an RF signal received by an antenna system (210, 410).

18. Method, according to claim 15, characterized by:

15 setting the reset signal while the input voltage is increasing from less than or equal to a minimum sustaining voltage (Vsustain) to a minimum starting voltage (Vstart), and

clearing the reset signal when the input voltage has increased above the minimum starting voltage.

19. Method, according to claim 18, characterized by:

20 clearing the reset signal after the input voltage has increased above the minimum starting voltage,

maintaining the cleared state of the reset signal while the input voltage remains above the minimum sustaining voltage; and

25 after the input voltage increases above the minimum starting voltage, setting the reset signal when the input voltage decreases to less than or equal to the minimum sustaining voltage, then maintaining the set state of the reset signal while the input voltage remains below the minimum starting voltage.

20. Method, according to claim 15, characterized by:

30 holding the reset signal in an ON-state after the beginning of power-up for a longer one of a first period of time which is a delay time (Ramp_Delay) and a second period of time which is a time expended while the input voltage increases to greater than a minimum voltage (Vsustain, Vstart).

21. Method, according to claim 13, characterized by:

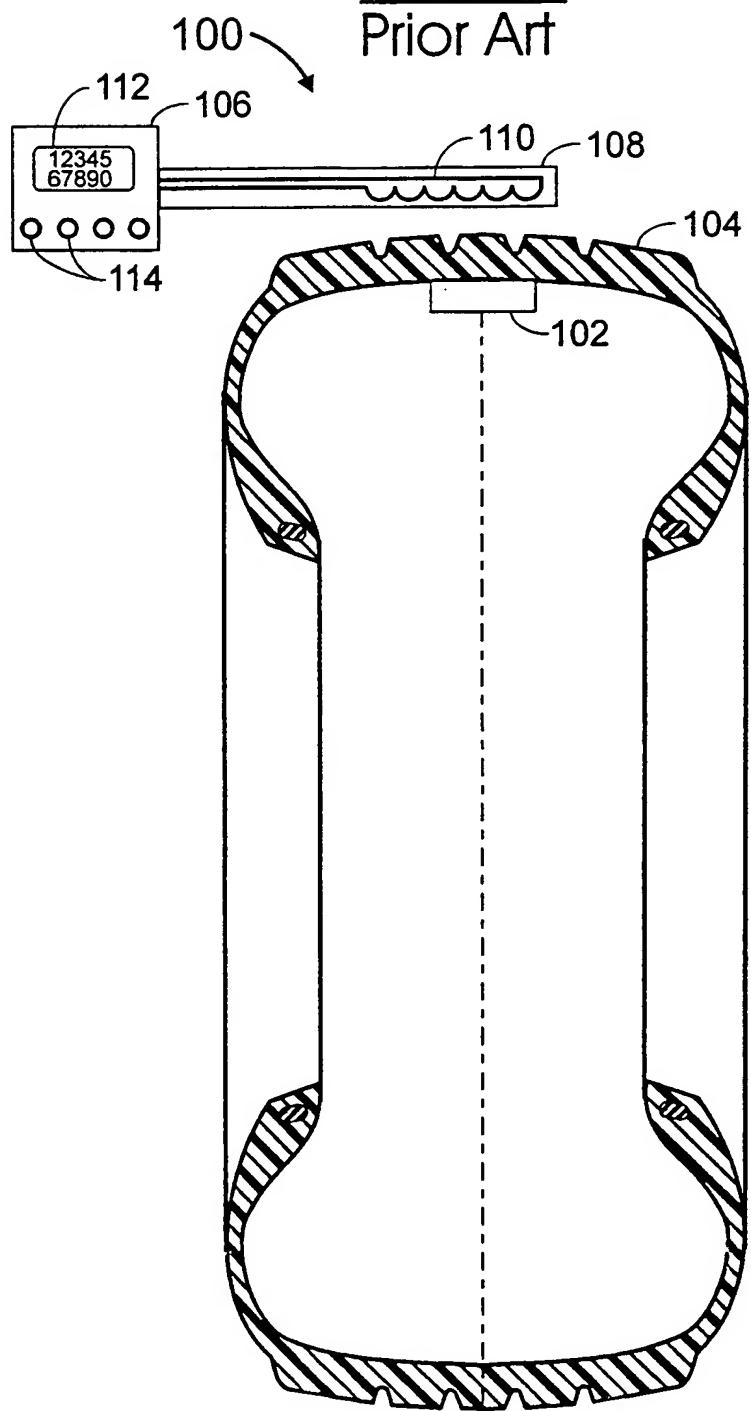
setting a combined reset signal (RESET) when either an externally-supplied reset signal (EXT_RES) or the transponder-generated reset signal (INT_RES) is set; and clearing the combined reset signal when both the external and the transponder-generated reset signals are clear.

5 22. Method, according to claim 21, characterized by:
 clearing the externally-supplied reset signal whenever the voltage level of the power supply is suitable for digital logic control.

23. Method, according to claim 13, characterized in that:
 the power for the transponder circuitry generating and releasing the reset
10 signal is the highest available regulated voltage (Vxx); and
 causing transponder circuitry which generates and releases the reset signal to
 be functional before the other ones of the plurality of circuits become functional.

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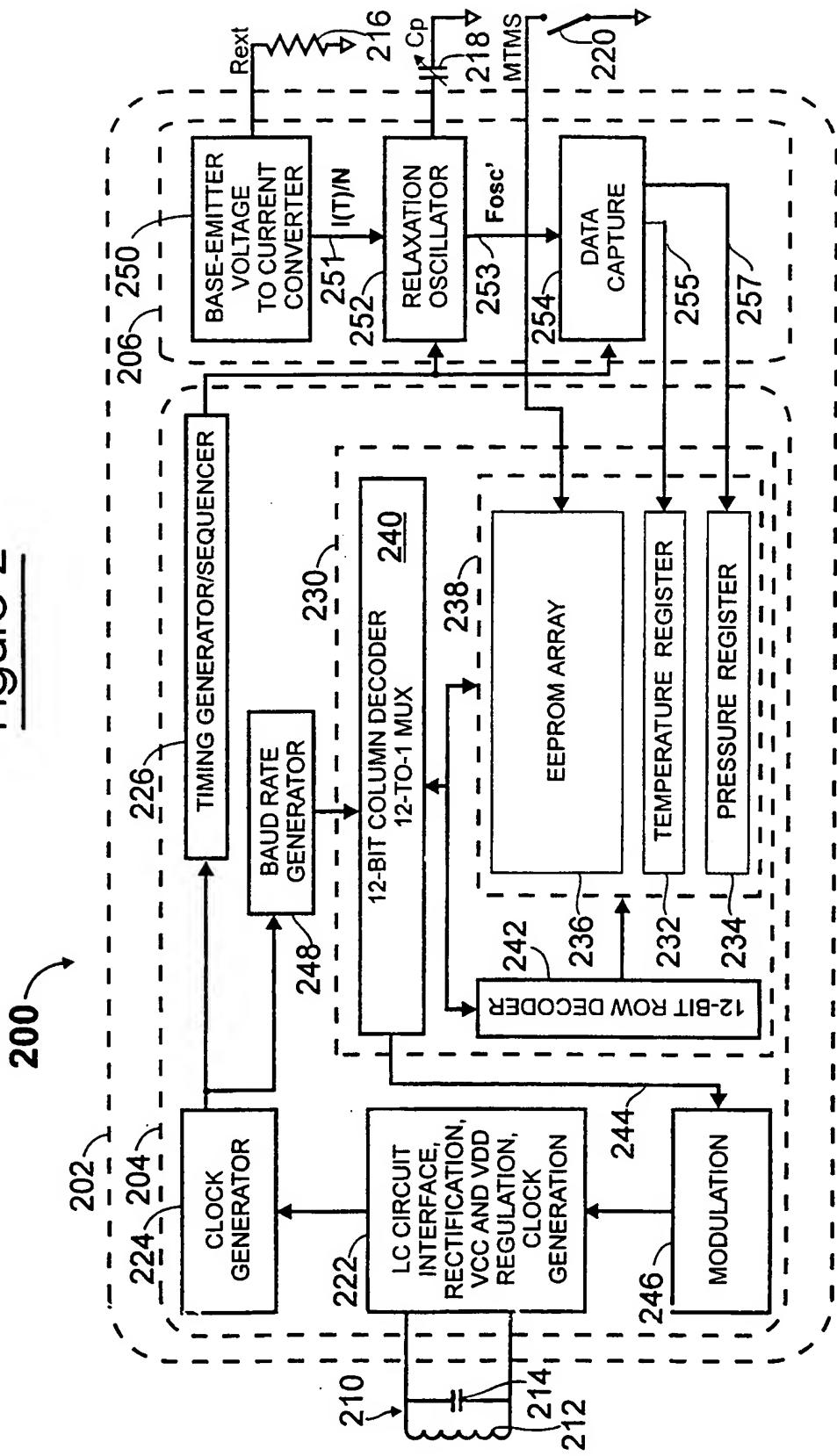
Figure 1
Prior Art



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Figure 2



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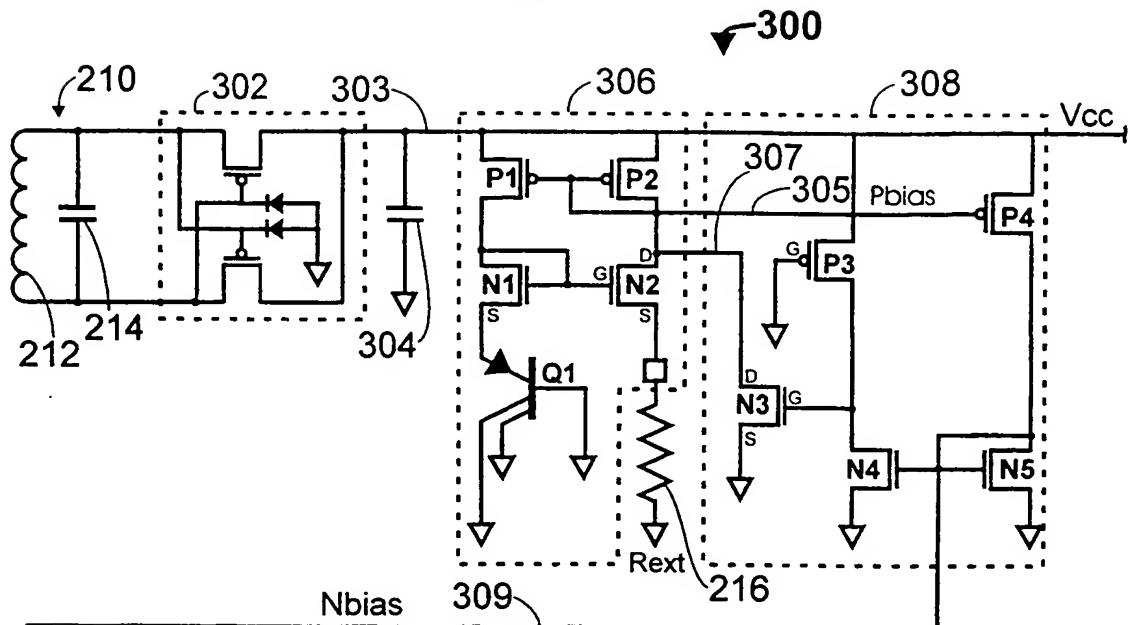
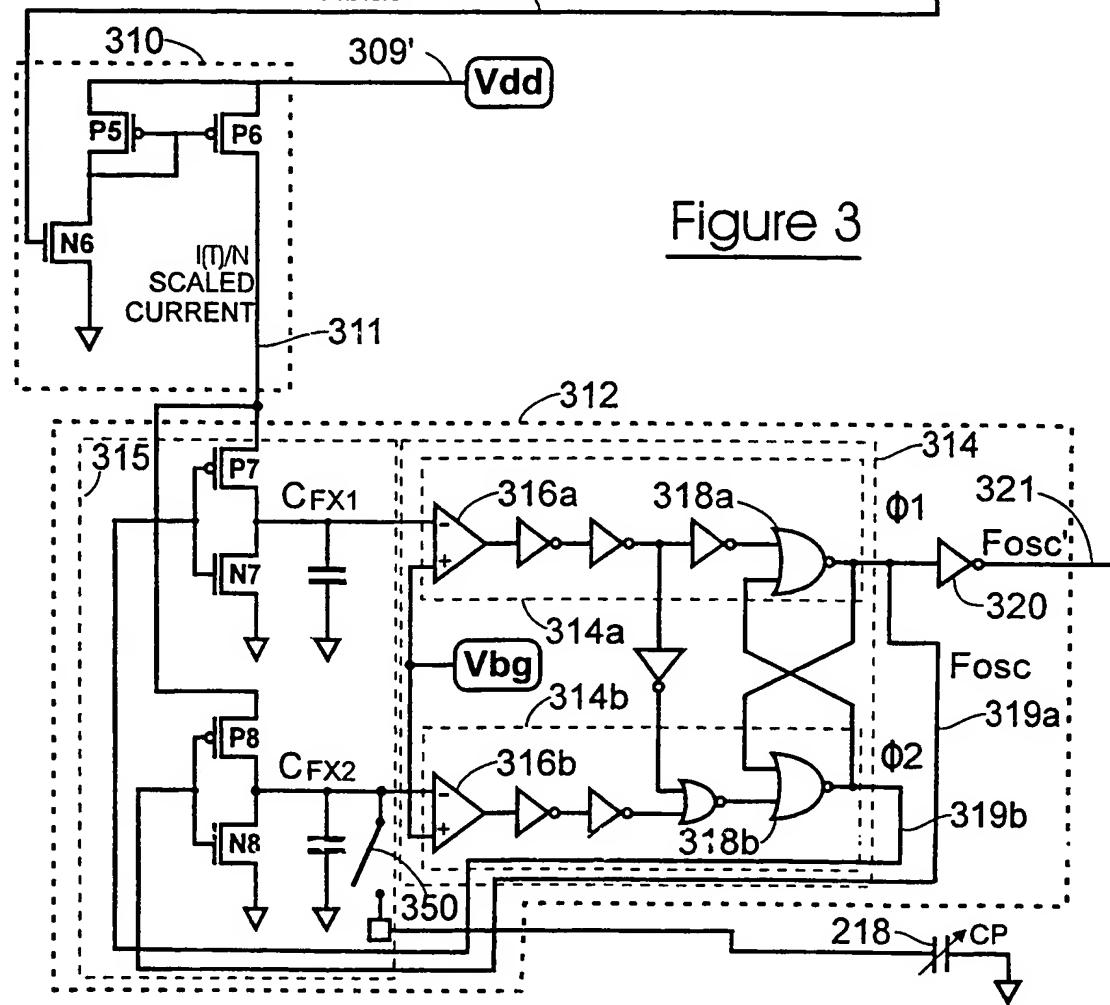
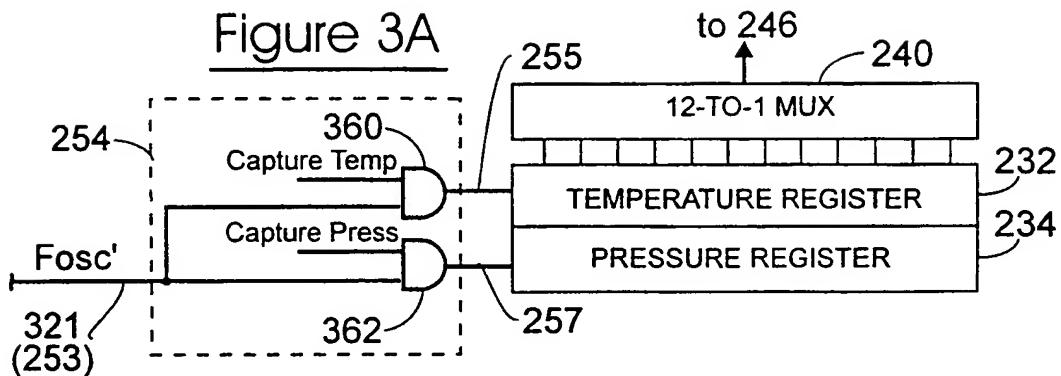
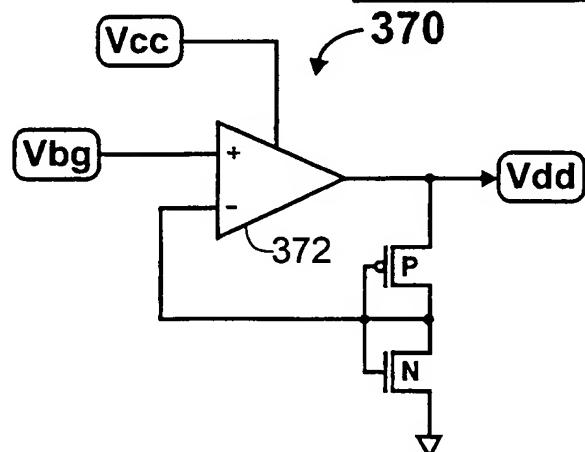


Figure 3



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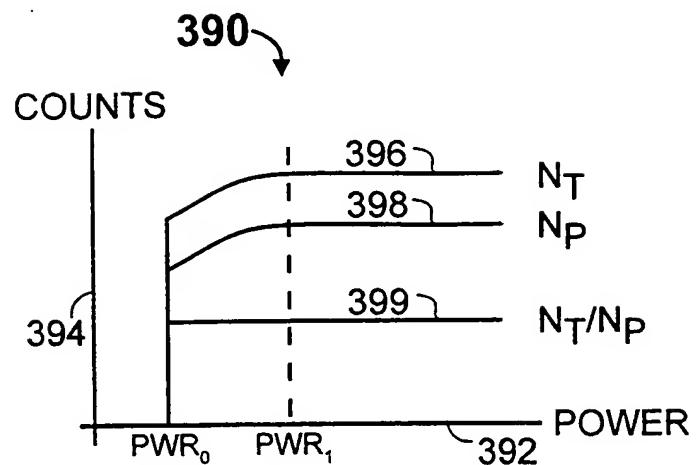
Figure 3AFigure 3BFigure 3C

← 12 COLUMNS →

ROW 1	SYNC 000..011
ROW 2	DATA 012..023
ROW 3	DATA 024..035
ROW 4	DATA 036..047
ROW 5	DATA 048..059
ROW 6	DATA 060..071
ROW 7	DATA 072..082, MTMS 083
ROW 8	TEMP COMP 084..095
ROW 9	PRESS COMP 096..107
ROW 10	TEMP/PRESS SLOPES 108..113, 114..119
ROW 11	TEMP COUNT (NT) 120..131
ROW 12	PRESS COUNT (NP) 132..143

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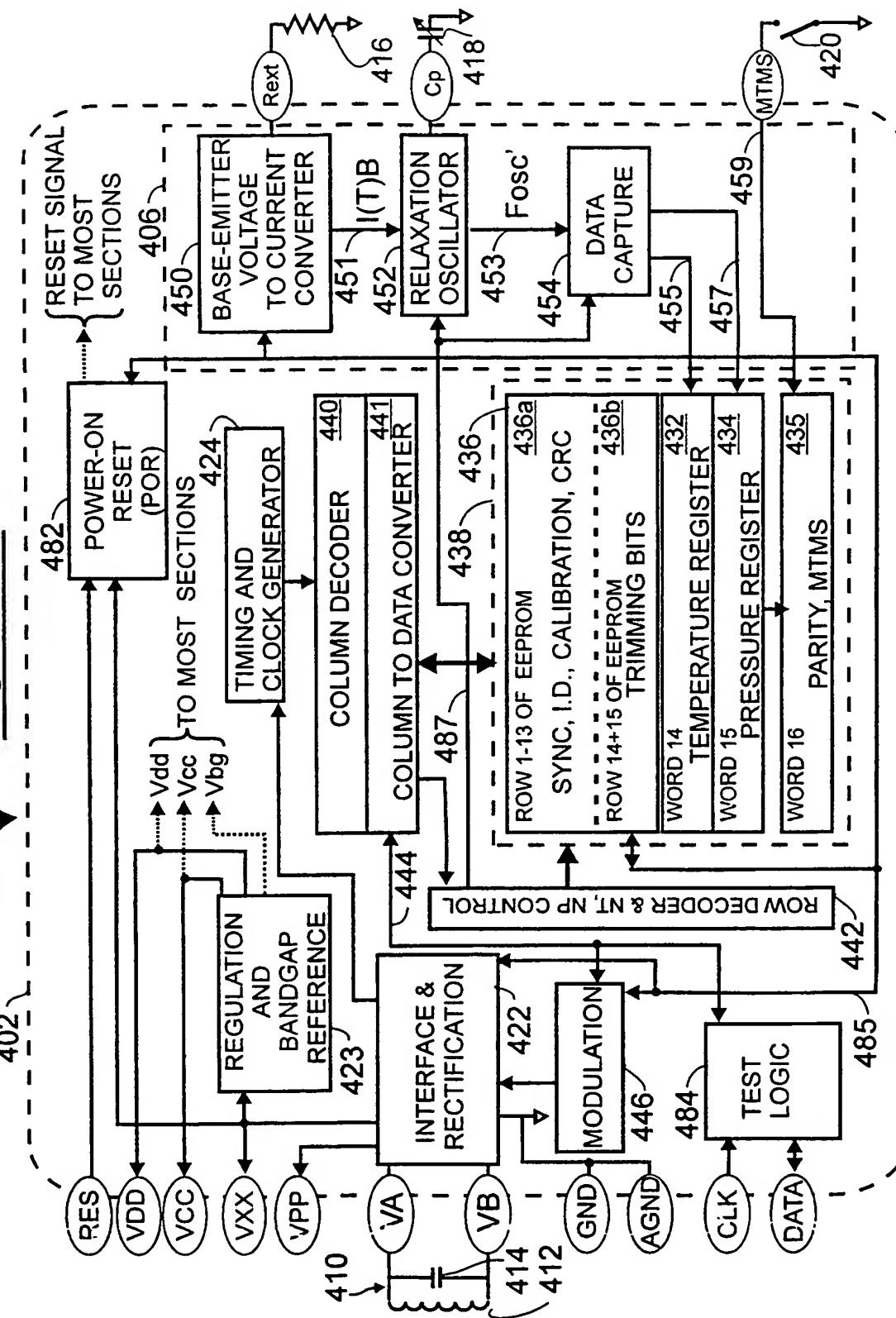
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Figure 3D

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Figure 4A



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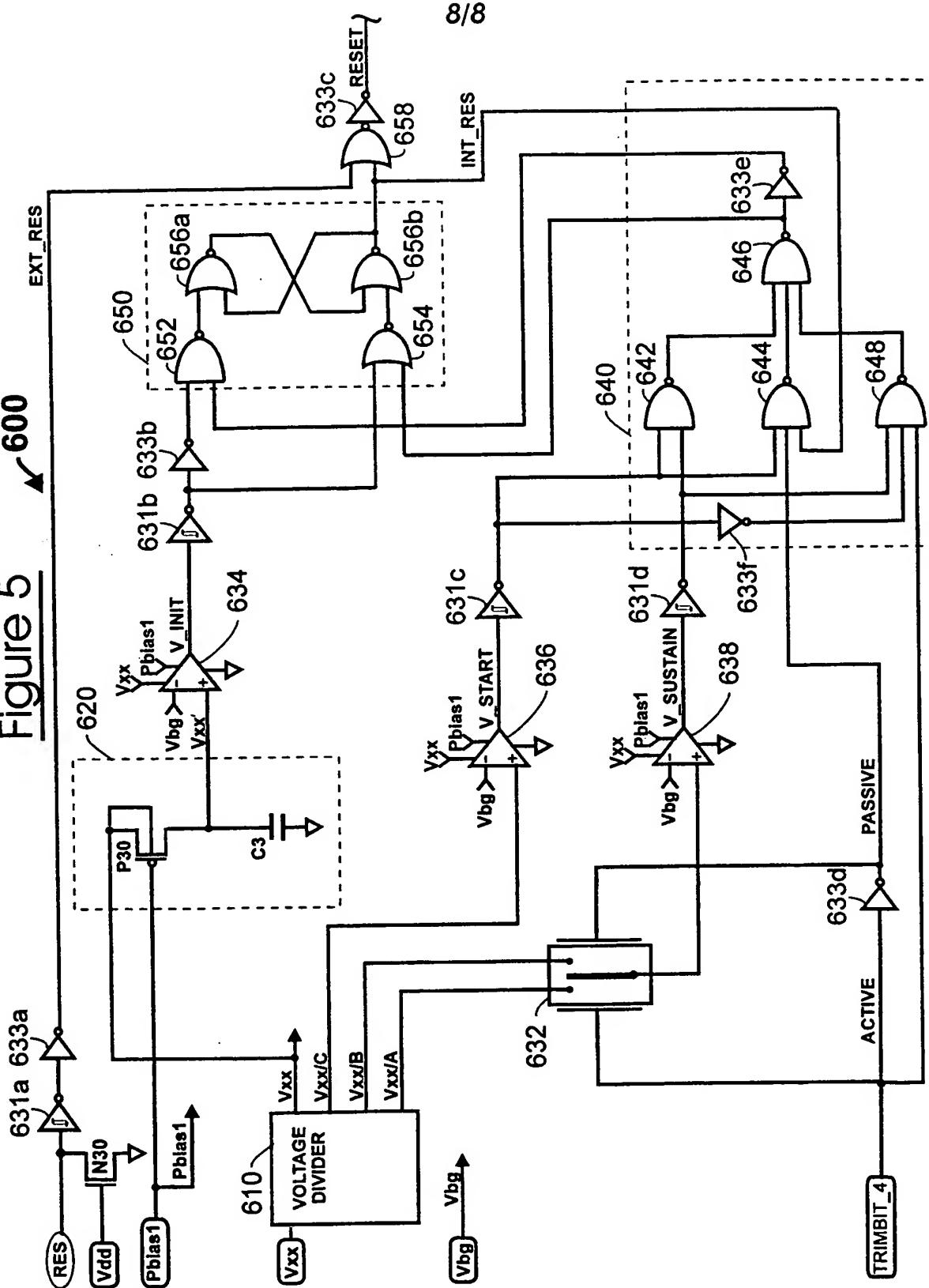
Figure 4B

EEPROM LOCATION	DATA STREAM	← 12-BIT WORDS →	
ROW 1	WORD 1	SYNC WORD (12)	12-BIT SYNC WORD
ROW 2	WORD 2	ID (12)	48 BITS OF USER ID
ROW 3	WORD 3	ID (12)	
ROW 4	WORD 4	ID (12)	
ROW 5	WORD 5	ID (12)	
ROW 6	WORD 6	TEMPERATURE CALIBRATION (12)	48 BITS OF TEMPERATURE & PRESSURE CALIBRATION DATA
ROW 7	WORD 7	TEMPERATURE CALIBRATION (12)	
ROW 8	WORD 8	PRESSURE CALIBRATION (12)	
ROW 9	WORD 9	PRESSURE CALIBRATION (12)	
ROW 10	WORD 10	CHIP ID (12)	36 BITS OF TRANSPONDER CHIP ID
ROW 11	WORD 11	CHIP ID (12)	
ROW 12	WORD 12	CHIP ID (12)	
ROW 13	WORD 13	CAL ID (4) CRC (8)	4-BIT CALIBRATION ID AND 8-BIT CRC
	WORD 14	TEMPERATURE NT (12)	TEMPERATURE (NT) AND PRESSURE (NP) DATA REGISTERS
	WORD 15	PRESSURE NP (12)	
	WORD 16	OPEN (5), MTMS(1) NP, NT PARITY(6)	11111, MTMS STATUS, AND PARITY OF NP, NT DATA
ROW 14		TRIMMING BITS (12)	12-BIT TRIMMING REGISTER
ROW 15		TRIMMING INVERSE BITS (12)	

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Figure 5 600

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/29723

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 B60C23/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 B60C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 832 765 A (MOTOROLA INC) 1 April 1998 (1998-04-01) column 7, line 2 -column 9, line 16; figures 3,5	1,13,15
A		2,3,9, 11,14, 16,18, 20,21,23
Y	US 5 824 891 A (MONSON MARK BRIAN) 20 October 1998 (1998-10-20) column 7, line 15 -column 8, line 63; figure 4	1,13,15

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents :

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- "E" earlier document but published on or after the International filing date
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"T" later document published after the International filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Z" document member of the same patent family

Date of the actual completion of the International search

Date of mailing of the International search report

23 March 2000

13/04/2000

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Smeijers, H

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern. Appl. No.

PCT/US 99/29723

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP 0832765	A 01-04-1998	JP 10111205 A US 5883305 A		28-04-1998 16-03-1999
US 5824891	A 20-10-1998	EP 0799728 A EP 0810108 A EP 0799729 A JP 10054770 A JP 10054771 A JP 10054772 A US 5844130 A US 5939977 A		08-10-1997 03-12-1997 08-10-1997 24-02-1998 24-02-1998 24-02-1998 01-12-1998 17-08-1999